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Suppressing ICs which have BGA packages or multiple DC power rails, 2013

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Suppressing ICs which have BGA packages and/or multiple DC power rails

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In the good old days all digital circuits were large black integrated circuits (ICs) with a row of 7, 8 or 10 pins on a 0.1 inch (2.54mm) pitch spread along each of their long edges. And they all ran on 5V DC power.

Well, there were exceptions to these rules even then, but the above statement will do to describe the devices most digital logic designers used on most days.

These days, ICs are still black(ish) but are often larger, can have 1000 or more pins in a gridded array covering most/all of one surface – where they cannot be reached by a soldering iron – known as Ball Grid Array (BGA) packaging. And they often need to be provided with several DC power rails.

These ICs can contain more than a billion transistors, and may, for example, be:

- Volume-manufactured multi-core microprocessors such as the Intel Core™ *i5* pictured in Figure 1
- Volume-manufactured memory ICs (DRAM, SDRAM, DDRAM, etc.)
- Volume-manufactured field programmable gate arrays (FPGAs) such as the Xilinx Vertex–7 pictured in Figure 2
- Custom-design application-specific integrated circuits (ASICs) such as the one codenamed JEKYLL developed by ON Semiconductor in collaboration with Airbus for their A350 XWB Flight Control Computer, see Figure 3.

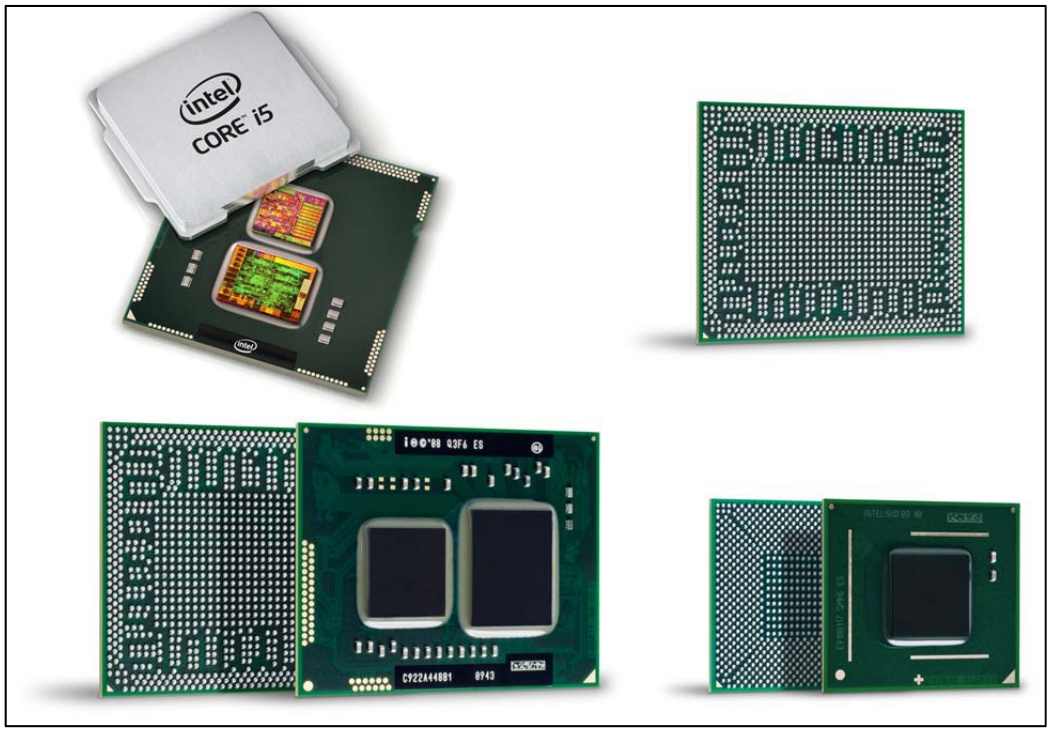

Figure 1 Example of an Intel Core™ *i5* microprocessor BGA

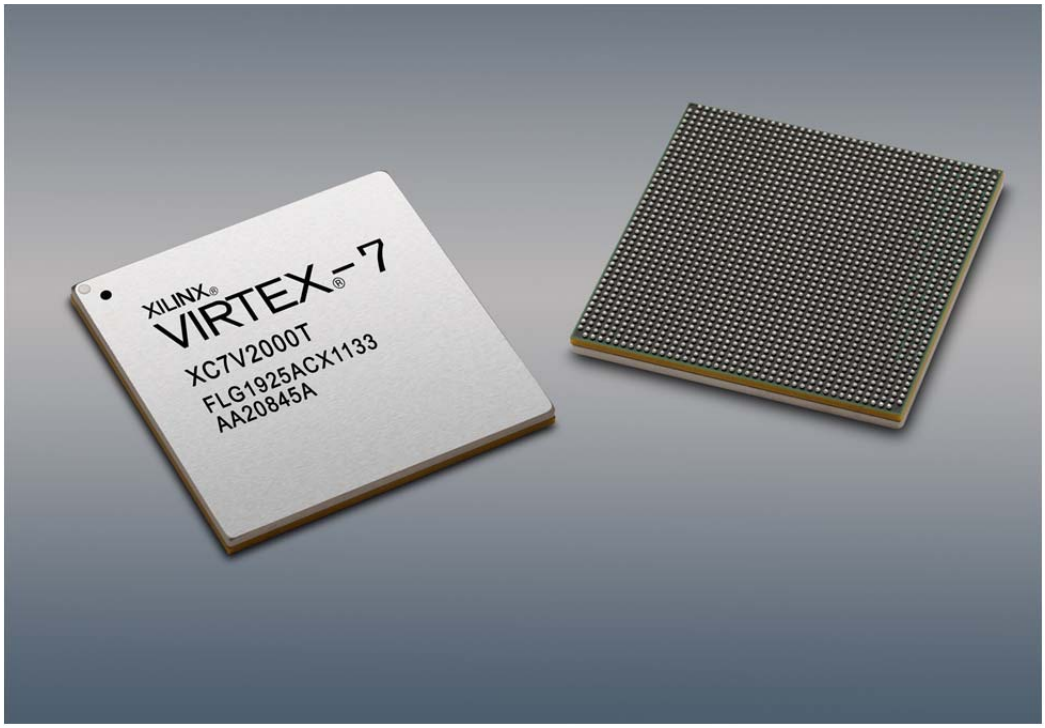

Figure 2 Example of a Xilinx FPGA in BGA packaging

Figure 3 ON Semiconductor's internal 110 nanometer (nm) process technology, using BGA packaging, that they use for ASICs

Most EMC design textbooks that cover printed circuit board (PCB) design (including mine [1] [2]) do not cover the EMC issues associated with BGAs, so I thought a brief article on suppressing them to reduce their emissions and increase their immunity might be of some interest.

Use HDI to ensure solid 0V and Power planes under BGAs

When using through-hole-plate (THP) PCB technology, the array of through-holes under BGAs makes it impossible to get solid (i.e. continuous, unbroken) copper planes under them – but the one place on a PCB where solid planes are needed the most for their EMC benefits is underneath the ICs!

The ideal solution is to use High-Density Interconnect (HDI) PCB technology because it does not use holes drilled through the entire thickness of the board – just those layers that need them – so 0V and Power planes can pass underneath an IC and remain solid, continuous, unbroken and unperforated by through-holes.

HDI board technology was originally developed so that 0V planes in cellphones could be solid copper sheets with no (few) perforations, and seems to be more often called 'Microvia' PCB technology. Other names for it include 'Build-up', because each layer is drilled and plated before lamination to create the complete PCB.

The basic standard on HDI is IPC-2315 (from www.ipc.org), and its benefits for EMC are discussed in section 7.5 of [2]. Figure 4 is a cross-section of an example six-layer board using this technology, showing its major features.

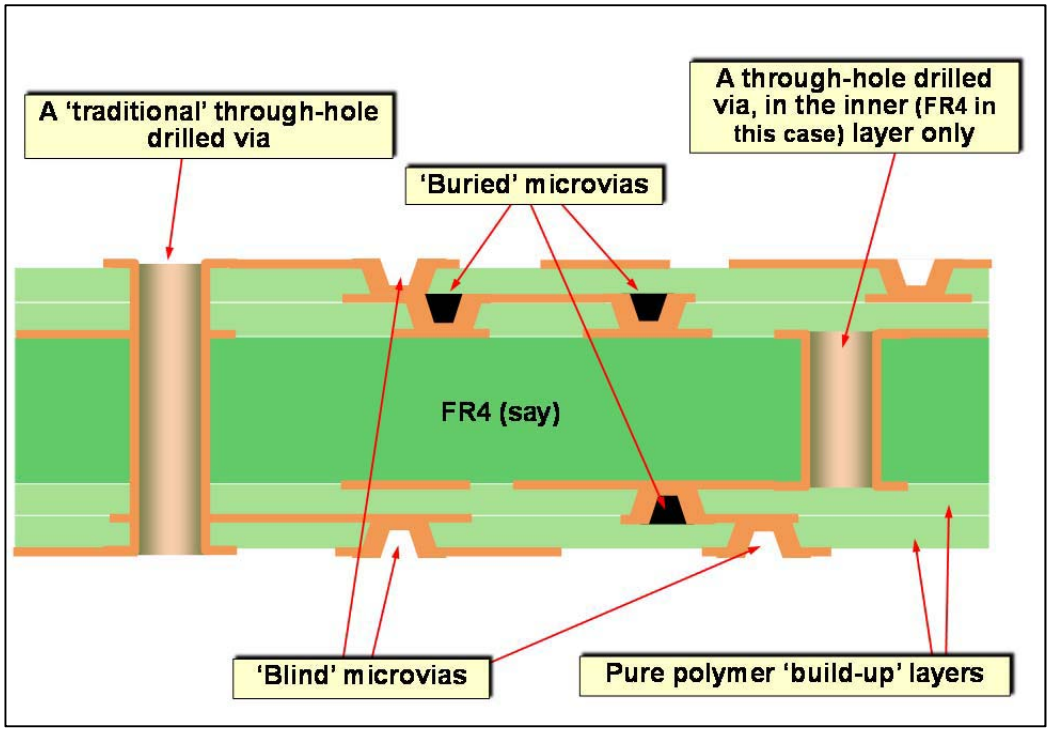

Figure 4 Example of a 6-layer HDI ('microvia') Xilinx FPGA in BGA packaging

The usual reaction when I suggest using HDI is horror at the cost of it – but this is an old-fashioned reaction that hasn't been true for well over a decade. An IPC (Institute of Printed Circuits) survey in 2000 found that HDI boards could be purchased for the same cost as THP, and if you can avoid the use of buried vias it helps reduce costs further.

Advice in recent years from Mentor Graphics' HDI expert Happy Holden is that boards needing more than 8-10 layers should cost less if made in HDI, for example a high-density 18 layer THP board would only need 10 layers if using HDI. But with even lower densities and with fewer layers, the EMC, signal integrity (SI) and power integrity (PI) advantages of HDI PCB technology can make it more cost-effective than boring old THP.

In May 2008 there were 32 manufacturers of microvia boards in the UK alone. HDI requires a different approach to PCB layout than THP, and some PCB EMC techniques might not be able to be used. Manufacturing techniques can vary between board manufacturers, and may need different layout techniques, so it is important to always check with the chosen manufacturer *before starting* board layout.

An important EMC advantage of microvia (HDI) PCB technology is that it's very small diameter individual-layer-piercing holes are closed off, so do not suck solder away from the joints on the top or bottom sides of the board, meaning they can be placed right in the middle of the BGA solder pads.

However, it is possible to use 'via-in-pad' techniques when using BGAs on THP PCBs, to save board area by avoiding the traditional 'dog-bone' pads, by filling or capping those vias with copper. In volume production this should add no more than 10% to the bare-board cost. To keep the price of prototypes down, these vias can be manually filled with high-melting-point solder before the board has its solder paste printed, components placed, and is passed through the solder reflow ovens.

At least use small enough track-and-gap rules to ensure meshed 0V and Power planes under BGAs

Using THP PCB technology inevitably means massive perforation of all 0V and Power planes under a BGA, which is bad for EMC.

I often see PCB designers using track-and-gap board layout rules that entirely remove *all* of the plane areas under BGAs – making SI, PI and EMC very difficult and costly to achieve and often delaying projects significantly (since 2000, delay is more important for a project than increases in BOM cost, see [3] and [4]) (BOM = Bill of Materials).

It is vital to at least achieve a continuous mesh (grid) in the 0V and Power planes under every BGA, to connect to all of the IC's 0V and Power pins to their respective DC supplies and decoupling capacitors ('decaps') with the lowest practicable impedance.

To create complete meshes or grids in planes underneath BGAs with ball pitches down to 1mm requires 175µm (7 thousands of an inch, or 'thou') or less track-and-gap rules.

Ball-pitches between 1mm and 0.8mm need 100µm (4 thou) or less track-and-gap; and 0.5mm pitch needs 50µm (2 thou) track-and-gap to maintain a complete mesh.

Figure 5 shows part of a signal layer under a BGA, in a multi-layer PCB with several 0V and Power planes. The BGA's 0V vias are shown as violet dots on the 0V plane fill, whereas power and signal vias are shown surrounded by a 100µm (4 thou) clearance holes in the 0V fill – sufficient to ensure that the 0V plane fill forms as complete a mesh (which has the lowest obtainable impedance) as practicable.

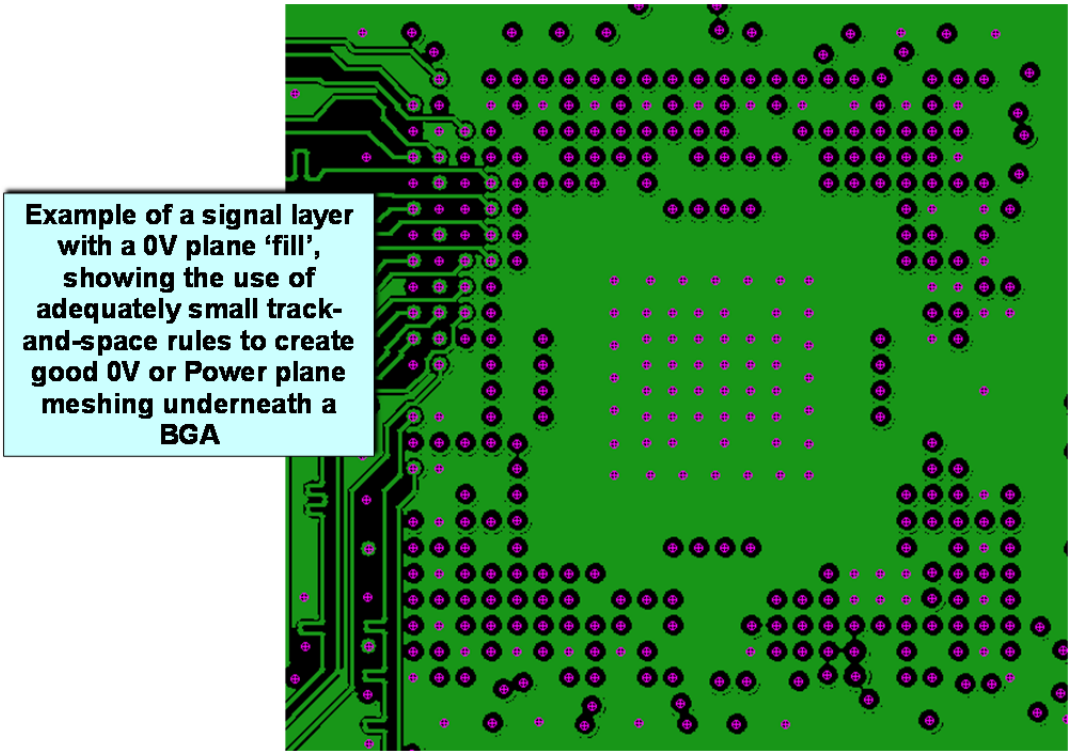

Figure 5 Example of a signal layer with a meshed 0V fill under a BGA

The problem with using too-large clearance holes in a plane is that they break into each other creating large gaps in the plane, considerably increasing its impedance. Figure 5 appears to show some pairs of clearance holes merging into each other to produce 'dumb-bell' shaped plane gaps, but this is due to the pixellation of the view I have chosen to use in this figure.

However, zooming in closer reveals that the 100µm (4 thou) clearance holes in the 0V fill do not break into each other, and a copper web of manufacturable thickness (at least 100µm (4 thou) wide) exists between any pairs of vias.

Once again, when I suggest using 175µm (7 thou) or less track-and-gap rules I often find people complaining about the price – but this size track-and-gap has been available with no price premium since before 2000.

And since about 2009 it has been very easy to purchase PCBs using 100µm (4 thou) track-and-gap from offshore volume-manufacturer with no price premium.

My experience seems to reveal that most company buyers form long-term relationships with their PCB suppliers, so that when a designer asks for a quotation based on 100µm (4 thou) track-and-gap they are given a higher price than they would expect for their normal design rules, which their manager then vetoes because he or she is still under the misapprehension that BOM cost is the most important issue.

As regular readers of my articles will know, such a veto is wrong in two major ways:

a) Suppressing EMI at PCB level is at least ten times less costly to the BOM of the final EMC-compliant product, and possibly 100 times or more less costly.

b) As already mentioned, time-to-market now dominates the financial success of a product [3].

For several years now, every customer suffering a delayed project because of poor EMC at least partly caused by gaping holes in the planes under their BGAs, to whom I have recommended the use of 100µm (4 thou) track-and-gap PCB design rules, has replied that it would be too expensive (but see a) and b) above). In every single case I strongly suggested they make their company buyer do his job properly and shop around, which they did, and found they could purchase such PCBs for no extra cost.

Everyone should realise by now that in this world as it is we can't get the best price unless we shop around. Sometimes the best price is from the very same supplier we have been using for years, who was hoping to rely on our loyalty to stay with them whatever price cuts they 'forgot' to offer us.

(Of course, this is not an argument for buying from non-approved suppliers, and especially not from the grey market! As an ancient Chinese proverb says (or so I have been told): the sweet taste of low cost does not last as long as the sour taste of poor quality. And when Confucius (or whoever) coined that saying, company buyers did not have to contend with the massive global fraud of counterfeit components that is run by organised crime that we have today.)

As for prototypes, there are UK PCB manufacturers who can cope down to 50µm (2 thou) track-and-gap (e.g. Merlin Circuit Technology), and I receive many emails each day from Chinese PCB manufacturers who used to only be interested in high volumes, but now offer very quick turnarounds and reasonable prices for prototype quantities of boards with almost any number of layers.

Suppressing ICs that have multiple power rails

Many microprocessors, FPGAs and ASICs now use multiple power supplies, such as 3.3V (for 'glue logic' I/Os), 2.5V and 2.7V (for different kinds of memory and other ICs) and between 1.2 and 0.9V for their core processing logic. They also use BGA packaging.

It helps a great deal if all of the different Power planes associated with an IC can be placed on a single PCB layer, with at least one adjacent 'solid' 0V plane in the PCB's layer stack, as shown in Figures 6 and 7.

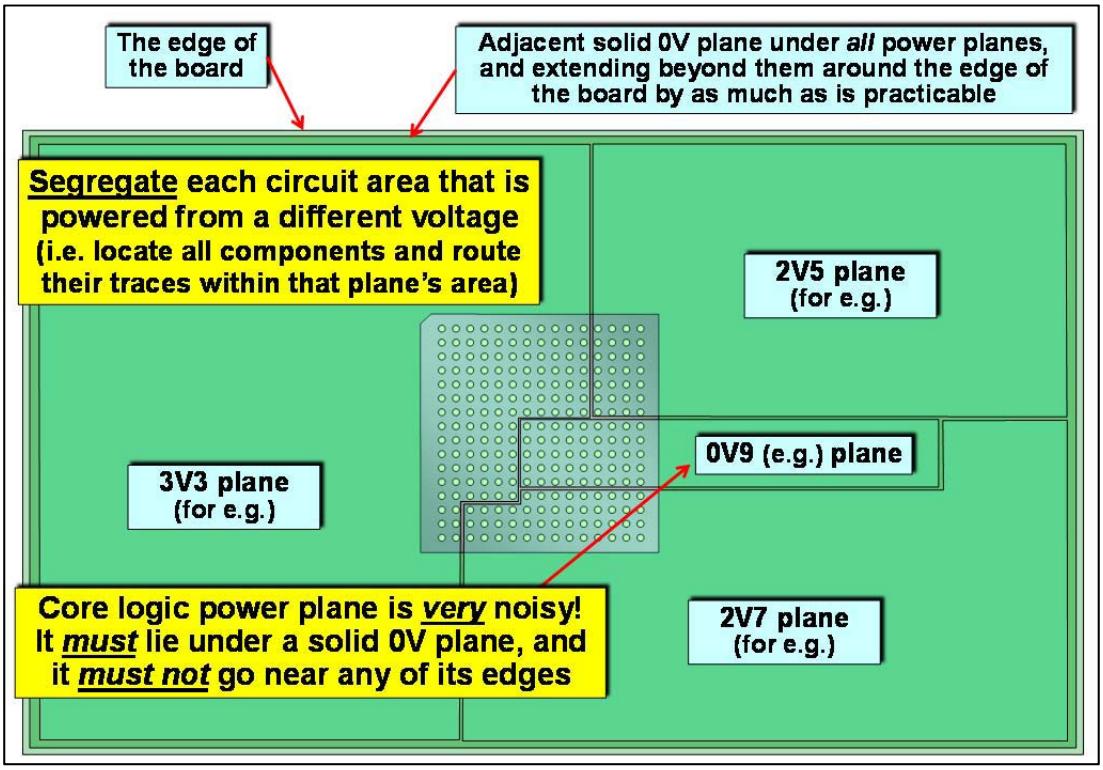

Figure 6 Overview of a Power plane layout for a BGA with four DC rails

Note that all of an IC's pins that are associated with the circuits that are powered from a given power rail voltage (e.g. 3,3V) are contained within that Power plane's area. This also applies to any unprogrammed pins on FPGAs, so that any future changes that bring these pins into use, doesn't require too many modifications to the layout and increase the risks of large changes to its EMC characteristics.

The spacing between the 0V plane and its adjacent split Power plane layer should be as small as is practicable. 50µm (2 thou) spacing is increasingly common, as is the use of proprietary double-sided copper laminates having much smaller dielectric thicknesses, even as low as 8µm (e.g. 'Faradflex', www.faradflex.com).

Such small 0V-Power plane spacings maximise their distributed decoupling capacitances, which helps maintain low power supply impedances above 300MHz (which can't be done with discrete decaps alone, see sections 7.5.3 and 7.5.4 in [1] and – for more detail – section 5.3 in [2]).

They also help ensure that return currents in the 0V plane flow very locally to the area covered by that Power plane area, helping to maintain segregation (reducing noise coupling, or crosstalk, between different circuit areas).

The adjacent 0V plane (and all other 0V planes in the board's layer stack) should extend beyond the perimeters of all Power planes – and also beyond all traces, pads and PCB-mounted components – by at least 3mm and *preferably much further*, whilst also keeping all PCB-mounted components as low-profile as possible (see [5], also sections 7.4.1 and 7.4.6 in [1] and – for more detail – 4.2.1 in [2]). A 0V plane 'moat' of 10mm or more width would be a good idea for suppression of EMI.

If there is a large hole routed in a PCB (never a good idea for EMC) it should also have a moat of at least 3mm of 0V plane around its inner perimeter.

This is another example of a good EMC technique that costs little when implemented at the bare-board level of assembly, which gives EMC benefits that are often much more costly to achieve at a higher level of assembly (e.g. the assembled PCB) but are often vetoed by managers who don't understand that what matters is the overall cost of manufacture of the EMC-compliant product, not the BOM for the assembled PCB prior to EMC testing.

Of course, I realise that the use of 0V plane moats means increasing PCB size overall, and/or increasing component density by using smaller components, more board layers, HDI technology, etc., all of which add cost. But this cost increase is acceptable as a way of reducing the overall design project's financial risks and (most probably) reducing the overall cost of manufacture too.

This is because this approach helps ensure that we don't find ourselves in the potentially financially ruinous situation of failing EMC compliance tests where the only solutions that can possibly work will cause time-to-market delays which could quite possibly kill the entire project (see [3] and [4]).

When using 0V/Power plane pairs as suggested above, the components associated with each of the DC power rails should be placed, and all their traces routed, over their associated Power plane areas, as Figure 7 tries to show.

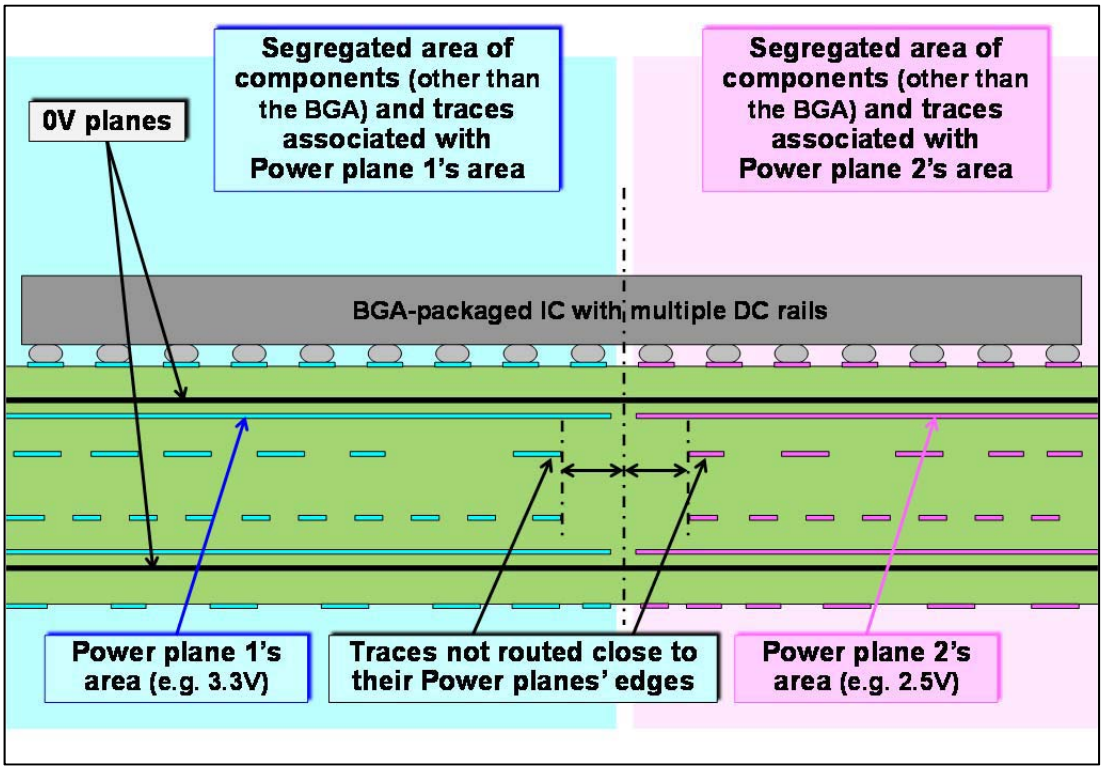

Figure 7 Example of segregating components and traces when a single Power plane layer is split into several DC plane areas

No traces that are routed on layers adjacent to any split Power plane layer(s) must ever cross any splits between plane areas on that layer, because the proportion of their return current that is flowing in the Power plane areas will not be controlled and will cause SI and PI problems, as well as problems for emissions and immunity.

(Almost all good EMC design engineering practices at RF can be reduced to the simple rule of providing paths for all 'return' currents (*including those caused by stray couplings*) that are physically very close indeed to the path taken by their 'send' currents, see [9], [6], [7] and [8].)

Just as for 0V planes, no traces should come too close to the edge of any Power plane area they are routed adjacent too (as shown by the double-headed arrows in Figure 7).

All traces that have to cross any plane splits (whether the splits are in 0V or Power planes) may need suppressing with filters, galvanic isolation, etc., see 4.4 in [2].

Segregating circuits into different areas of a PCB is a very important EMC technique, second only to the provision of solid (continuous, unbroken) 0V planes, and is described in section 7.2 of [1] and section 2 of [2].

Unfortunately, an IC with multiple DC power rails belongs to each of the segregated PCB areas associated with its split Power planes, which rather limits the usefulness of PCB-level shielding of those areas. But in real life engineering we can't have everything (unfortunately)!

Sometimes it is impractical to confine all of the Power planes to a single layer in a PCB, for example when a board has multiple-power-rail ICs mounted on one or both sides. For example, one of my customers had so many large FPGAs on both sides of a PCB that it needed four Power plane layers, each layer being split into several Power plane areas.

A problem here is that stray capacitance and stray inductance between plane layers causes noise to be coupled between them (crosstalk). So, for example, very high frequency noises associated with 2.5V DDR memory busses could couple into the 'ordinary' 3.3V Power planes and circulate in their associated circuitry, causing bad PI which leads to bad SI, and worse EMC.

Core logic Power planes (typically between 0.8V and 1.2V) are often the principal culprits in such situations. The current and voltage noises in these planes are usually extreme in both magnitude (Amps, sometimes tens of Amps) and frequency (at least up to 10GHz), and a physically small core logic Power plane can easily 'pollute' an entire PCB and all the cables it is connected to with RF noise, causing major problems for SI and PI, and of course for EMC.

To help prevent RF noise in a 'noisy' Power plane layer (e.g. a processor core logic supply) from coupling noise into a parallel Power plane layer and spreading more widely, causing higher emissions – place a 0V plane between them in the layer stack, as shown in Figure 8.

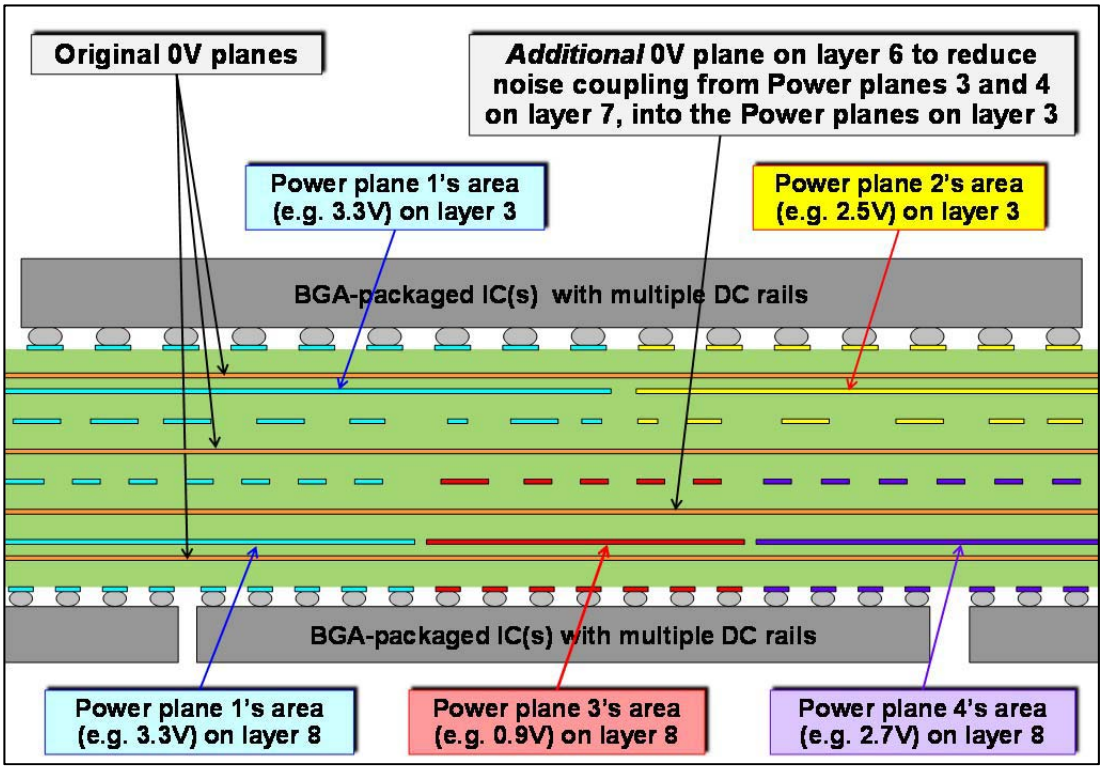

Figure 8 Example of adding a 0V layer to reduce the noise coupling between parallel Power plane layers at different voltages

'Sandwiching' each board layer that contains split Power plane areas between two solid (i.e. continuous, unbroken) 0V planes (e.g. as was done for layers 7, 8 and 9 in Figure 8) also has the benefit of increasing the Power planes' buried decoupling capacitances. And a still further benefit is that no signal traces have to avoid any splits in any planes, easing the constraints on signal layer routing at the cost of additional board layers.

I can see a day in the near future when it becomes standard board layout practice to sandwich every layer that contains split Power planes between two solid 0V planes.

Conclusions

ICs with BGA packaging and/or multiple DC power supplies are now unavoidable for many product designs, but attention to several issues associated with the 0V and Power planes in their PCB layouts will reduce their negative effects on SI, PI and EMC.

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