# PCB Design of Gb-s Differential Lines, July 2006



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# PCB Design Techniques for the SI and EMC of Gb/s Differential Transmission Lines

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**Abstract**

Differential transmission lines are becoming very common on printed circuit boards (PCBs), for carrying serial data at Gigabit/second (Gb/s) rates.

It is usually assumed that the electromagnetic compatibility (EMC) of such transmission lines will be better than the single-ended lines they replace – but in fact their EMC can easily be degraded by typical PCB design and routing techniques – to the point where it can be little better than that of single-ended lines.

This paper presents an overview of the PCB design problems and their solutions for maximising the EMC of differential transmission lines operating at all data rates up to Gb/s. No new work is presented, but the references are very recent and this paper presents the techniques all in one place, in a style that can be understood and used by PCB designers.

## Introduction

Balanced signalling (also called differential signalling) uses two conductors driven with antiphase signals, see Figure 1, and is increasingly required for clocks and data communications (e.g. USB2.0, Firewire, PCI Express [1]) for reasons of both signal integrity (SI) and EMC. As the name 'balanced' implies, a lack of balance (an imbalance) in the signalling degrades its SI and EMC performance, and the causes and solutions of imbalances are the subject of this paper.

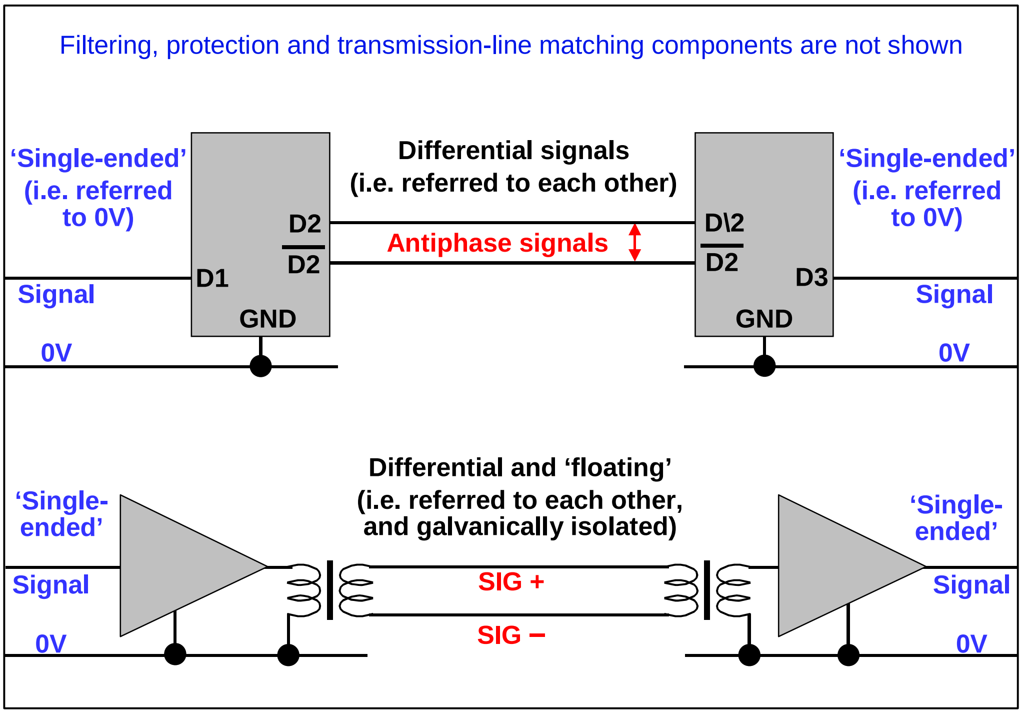



**Fig. 1 Two examples of balanced (differential) signalling circuits**

The general design of transmission lines, including differential ones, is described in [2], [3] and [4]. A wide variety of differential lines can be constructed using PCB traces and planes, and Figure 2 shows some of them.

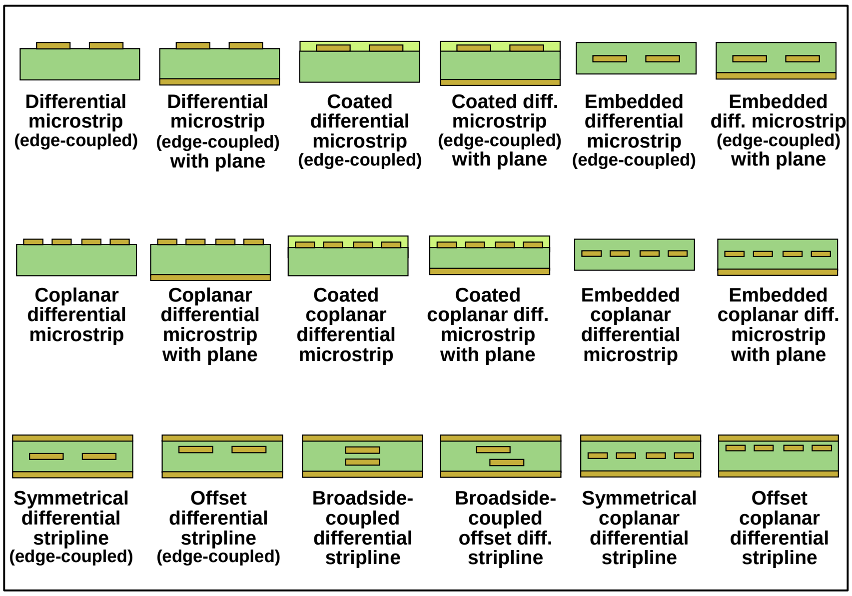



**Fig. 2 Some differential transmission line structures for PCBs**

For the best SI and EMC, closely-coupled trace pair lines should be routed symmetrically along their entire route, with both their differential-mode (DM) characteristic impedance $Z_{0DM}$ and their common-mode (CM) characteristic impedance $Z_{0CM}$ maintained along their length and terminated in a matched impedance at one end (preferably at both ends). LVDS receivers that accommodate a wide range of input levels allow the use of transmission line terminations at both ends.

A PCB plane along the trace pair's route, linking the driver's reference to the receiver's, provides a low-impedance return path for the inevitable CM noise currents caused by imbalances in the line, helping to improve EMC despite those imbalances. This plane should be unbroken (not split), and is usually the 0V reference. If the trace pair connects to a shielded cable, for the best EMC a low-impedance CM current return path should be provided by bonding the cable shield in 360° (a complete peripheral electrical connection all around its circumference) to the appropriate plane. (Note that good EMC also requires that both ends of the cable use 360° bonding.) Imbalances cause some of the DM (i.e. wanted) signal currents to be converted into unwanted CM noise currents [5] (see Figure 3) that cause emissions. In SI terms, imbalances in a differential trace pair causes the data 'eye pattern' to close.

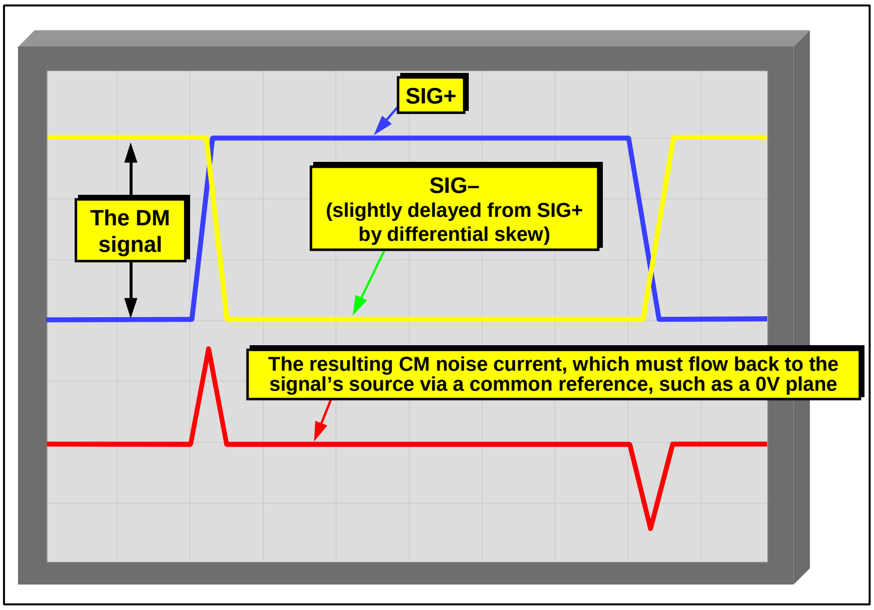



**Fig. 3 DM signals are partially converted into common-mode (CM) noise by differential skew**

Imbalances also cause degraded immunity, because they cause a proportion of the CM noise in the environment to be converted into DM noise in the trace pairs, where it can interfere with the correct operation of the circuit or software.

The main causes of imbalance can be arranged into three main groups:

- Differences in the trace pair's $Z_{0DM}$ or $Z_{0CM}$ along their route.
- Differential skew caused by different propagation times between the traces in a pair.
- Output impedances and timing skew of the drivers, and the accuracy of the matching of the $Z_{0DM}$ and $Z_{0CM}$ terminations over the frequency range. These issues do not affect the PCB layout, so are not covered in this paper.

PCB design features that have a significant effect on the $Z_{0DM}$ or $Z_{0CM}$ along a trace pair will often also affect differential skew, and vice-versa.

If there is a poor (i.e. high-impedance) path for the CM current from driver to receiver – for example if the trace pair is routed over a plane gap or split, a differential skew that is as large as the signals' rise/fall times can make the emissions from a differential line as bad as from a 'single-ended' line. [17] claims that intra-pair skew as large as 80ps makes differential routing no longer effective for preventing interference to wireless data communications, creating emissions similar to those from a single-ended trace. CM chokes can help mitigate the effects of imbalance, but consume space and are relatively expensive parts.

The remainder of this paper discusses what PCB issues cause imbalance, plus techniques to help control them.

### Unequal strays

Every signal conductor experiences stray capacitive and mutual inductance coupling to other conductors and conductive objects. Close proximity of materials with a high dielectric constant and/or high relative permeability will increase these strays. When a differential trace pair passes near an object, each trace will experience slightly different strays, causing imbalances and changes in the $Z_{0DM}$ or $Z_{0CM}$ along the trace pair. Figure 4 shows some typical PCB structures that cause unbalanced strays, including:

- Gaps in the substrate; PCB edges
- Gaps in planes; plane edges
- Objects made of metal, plastic, glass, ceramic, etc.
- Nearby traces or areas of copper fill
- Water (e.g. condensation), oil or other liquids

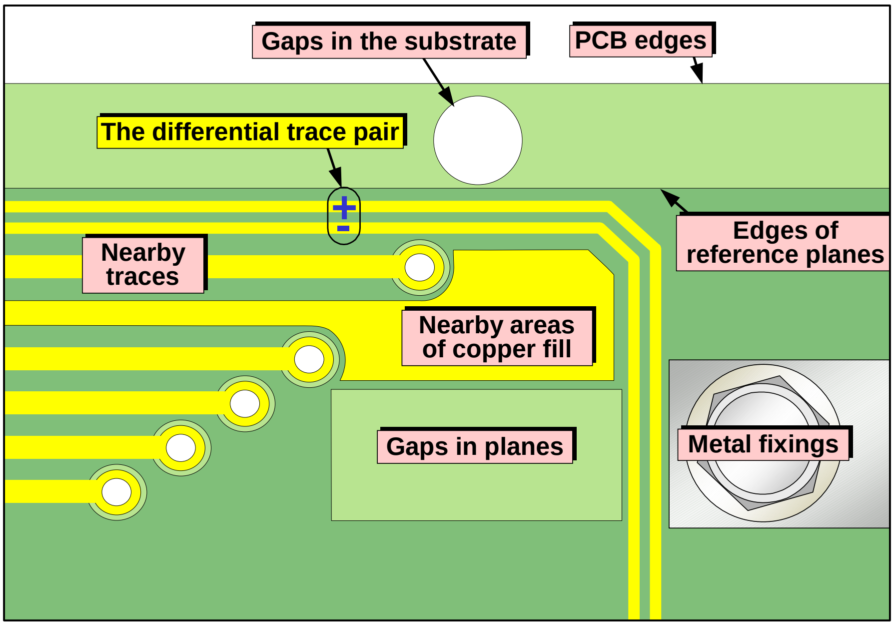



**Fig. 4 Examples of unbalanced strays**

To maintain good balance, trace pairs should be routed well away from anything that might cause unbalanced stray capacitance or mutual inductance. Recommended layouts for such situations exist (e.g. [6]) but most are concerned with SI - for good EMC stray imbalances must be much lower.

Unbalanced strays can be partially controlled using stripline traces between two unbroken planes, with vias linking the planes at least every tenth of the wavelength at the highest frequency of concern, over their whole area. Where the planes are at different potentials, decoupling capacitors should be used instead of vias. The planes and vias 'shield' the trace pair from objects and gaps or edges; using the same technique with coplanar striplines will be even better.

This technique can be extended by using a row of via holes routed symmetrically along both sides of a stripline trace pair (sometimes called 'via walls'), connected to the planes above and below as shown in Figure 5, to effectively create a shielded trace pair inside the PCB. When using a coplanar differential stripline the via rows should follow the routes of the outer (return) traces, linking them to the top and bottom planes. To provide significant shielding, the via holes in the walls must be no further apart than one-tenth of the wavelength at the highest frequency of concern, preferably much less.

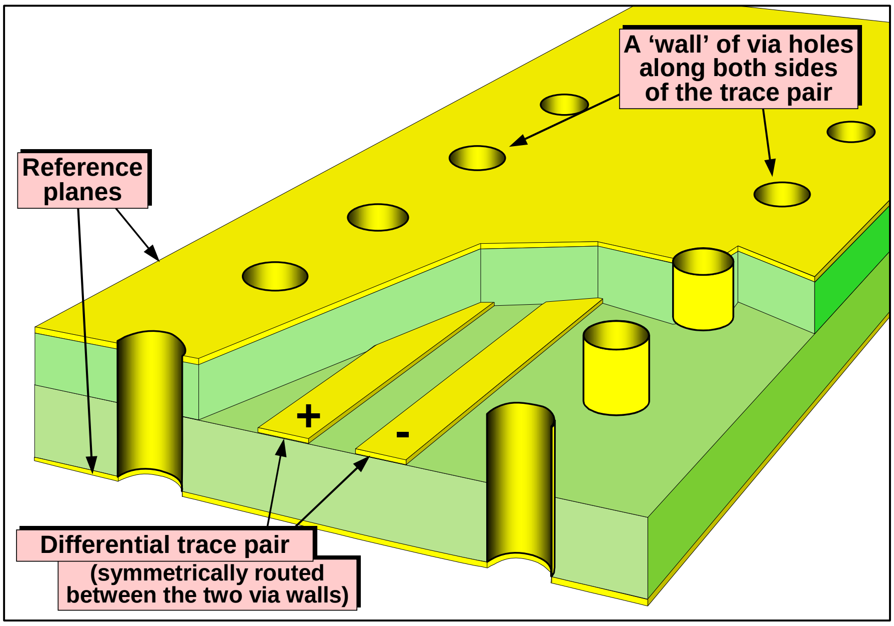
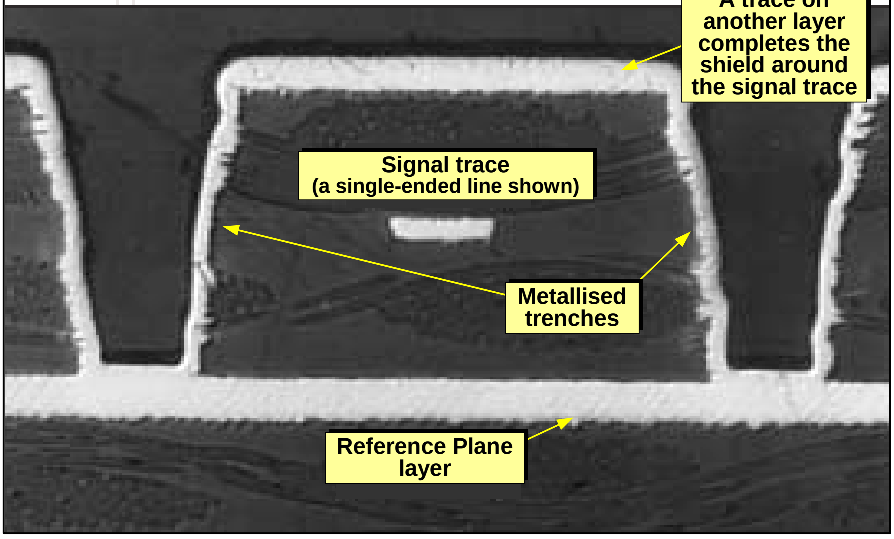



**Fig. 5 A shielded differential stripline**

It is possible to cut trenches between layers, plate them and back-fill them with epoxy, to create fully shielded trace pairs [7]. Figure 6 shows this technique applied to a single trace.




Taken from "Micro-Machining of Trenches to Form Shielded Transmission Lines", by Joan Tourne, Printed Circuit Design & Manufacture, April 2004, pp 34-3

**Fig. 6 Trace shielding with metallised trenches and planes**

Applying shielding to striplines as shown in Figures 5 and 6 is very effective at reducing the imbalances caused by nearby objects, gaps or edges. It also significantly improves the degraded emissions and immunity performances caused by other imbalances (discussed below). But shielding cannot affect imbalance problems that affect SI, so a low enough imbalance is still required for the trace pair *within* the shielding structure in the PCB. Also, it is important to note that adding shielding to a trace adds a distributed capacitance that reduces $Z_{0DM}$, $Z_{0CM}$ and $V$, so the usual formulae for these will not apply.

### Variations in trace widths

Differences between the widths of the traces in a pair are a cause of imbalance, and can be caused by process variations over the area of the PCB during manufacture. To help prevent this add 'test traces' [8] at two or more widely-separated locations on a PCB, so that manufacturing quality can be checked as part of a goods acceptance procedure. Differential test traces require a 4-port vector network analyser, and models suitable for non-expert use are available from manufacturers such as Polar Instruments.

Trace width differences and variations in the spacing of a pair can also occur, causing imbalances, depending on where the traces fall on the phototool's digitisation grid. Routing trace pairs between 20° and 70° with respect to the digitisation grid helps 'average out' these errors.

### Path length differences

Differences between the path lengths of the traces in a pair cause a difference in the propagation times between their + and – signals, see Figure 7, contributing to the overall differential skew of the trace pair.

For example: LVDS differential drivers with rise and fall times around 100ps are used in modern computer motherboards, and their rise and fall times are equivalent to a path length of about 15mm for a stripline using an FR4 PCB dielectric. So for good EMC where there is a poor (i.e. high-impedance) return path for CM currents from the receiver to the driver, the *overall* differential skew of their differential pairs should be no more than about one-tenth of their rise/fall times (10ps), which is equivalent to a path length difference of 1.5mm. However, path length differences are only one of several contributors to the overall differential skew, so when laying out a PCB the path length differences will probably need to be controlled to be much less than 1.5mm.

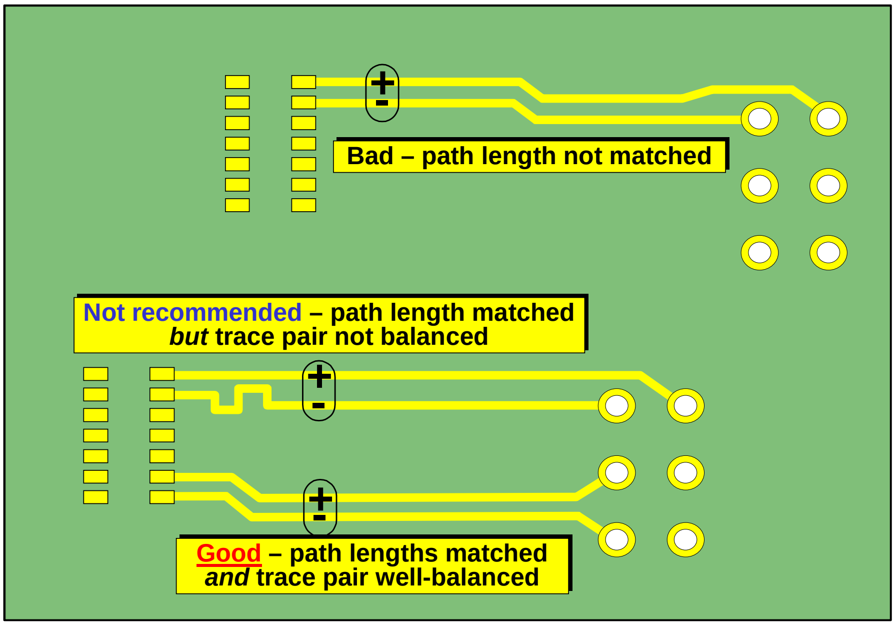



**Fig. 7 Maintain the same path length for each trace in a pair**

### Routing trace pairs in dense fields of pads or via holes

Dense fields of pads or vias cause difficulties for the symmetrical (balanced) routing of a trace pair, and can be a cause of imbalances. The best technique for dealing with this problem is to use trace widths and spacings as small as are required to route the trace pair symmetrically through the via field [9], as shown in Figure 8 – with a sufficient width of plane symmetrically routed on an adjacent layer in the stack-up for its CM return current path [10]. Microvia PCB technology (also known as high-density interconnect, or HDI) is recommended because its vias have very small diameters and do not penetrate every layer, making via fields less dense and making it easier to route trace pairs symmetrically.

Another technique is to space the traces in a pair so widely apart that their $Z_{0CM}$ is simply twice their $Z_{0DM}$ – then route them as individual traces along their whole route and through the via field, keeping the layout for each one identical as far as possible. This technique is also shown on Figure 8.

It may be possible to compensate for an imbalance in one trace in a pair, or a variation in the $Z_{0DM}$, by locally varying the width of one or both of the traces. Where the traces in a pair are widely separated this might be quite successful, but where a trace pair is closely coupled (routed closely together) – the best routing for good EMC – it will be more difficult to use this compensation technique whilst maintaining both $Z_{0DM}$ *and* $Z_{0CM}$ at the same time.

Routing two traces in parallel on adjacent layers is known as broadside routing, and is generally considered a poor technique [11] because inevitable variations in aligning the layers when physically constructing a PCB's stack-up result in changed line characteristics. But when routing through a field of vias it allows the traces to maintain their relationship with each other whilst routing only one trace between each pair of vias on any layer, see Figure 8, so it might be the 'least-worst' cost-effective solution in some situations.

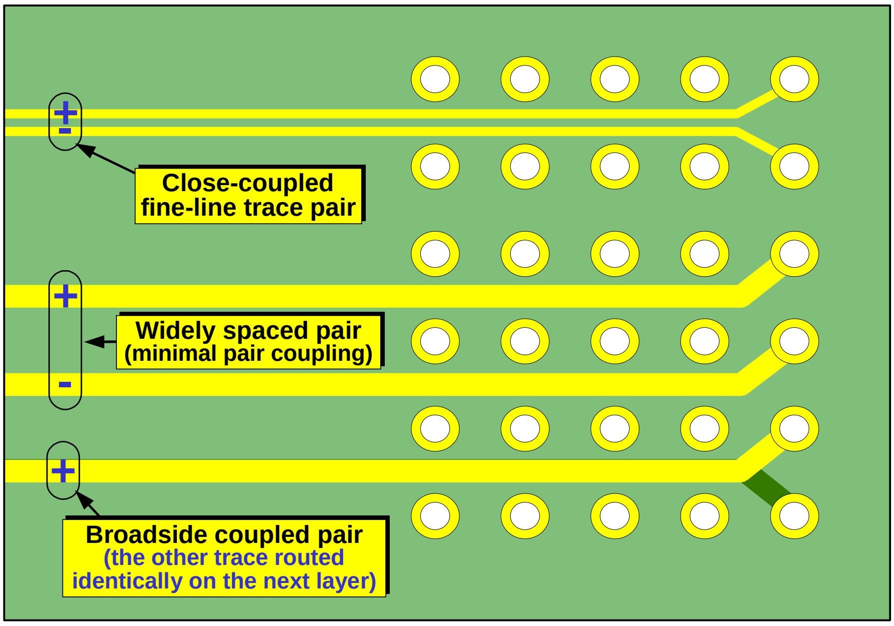



**Fig. 8 Maintaining balance when routing through a dense field of vias**

### Changing layers within a stack-up

Changing layers within a PCB's stack-up, by means of via holes, makes it extremely difficult to control $Z_{0DM}$ and $Z_{0CM}$ for a trace pair, and any unused lengths of via holes can create problems too [2] [12] by acting as band-reject filters for the signals or data on the pair. For the best SI and EMC, all Gb/s differential transmission lines on PCBs should be routed 'point-to-point' with no layer changes along their route (except where they connect to the driver and receiver at their ends). In practice, this is best achieved by first routing the decoupling, then routing the Gb/s trace pairs on single layers, then routing the other traces.

To prevent the layer changes at the ends of the trace pairs from causing EMC problems, the propagation times from the trace on its own layer to the actual transistors of the driver or receiver should be less than one-tenth of the actual rise/fall time (not the data sheet value). For example: if the real-life rise/fall time was 100ps, the overall length of the PCB's via hole plus the subsequent 'solder side' trace and pad, plus the IC's leadframe, bond wire and silicon metallisation, should be less than 1.5mm.

Some designers prefer to avoid the problems of layer changing by routing their trace pairs as microstrip lines. Unfortunately, microstrip is not as good as stripline for EMC, and cannot be 'shielded' as described earlier. Also, microstrip suffers from some causes of imbalance that do not afflict striplines, as described later.

### Glass-fibre PCB dielectrics

The glass-fibres in PCB dielectrics like FR4 have a much higher dielectric constant than the epoxy resin they are embedded in. As Figure 9 shows, the glass-fibres are woven like ordinary cloth and if a trace lies predominantly in/over a glass-rich area its $Z_0$ and $V$ will be lower than calculated. However, if a trace lies predominantly in/over an epoxy-rich area, its $Z_0$ and $V$ will be higher than calculated. Differential skews of up to 5% of the overall trace propagation time can be caused in this way [13].

One way of dealing with this is to route trace pairs at between 30° and 60° to the direction of the glass-fibres, ideally 45°, to help 'average out' the effects of the weave [14].

Another is to use homogenous PCB dielectrics instead of glass-fibre types, and [13] suggests that this may prove to be essential at data rates of 10Gb/s and above or with traces longer than 600mm. But homogenous dielectrics are more costly than glass-fibre types, so there is great pressure to develop ways to continue using woven types.

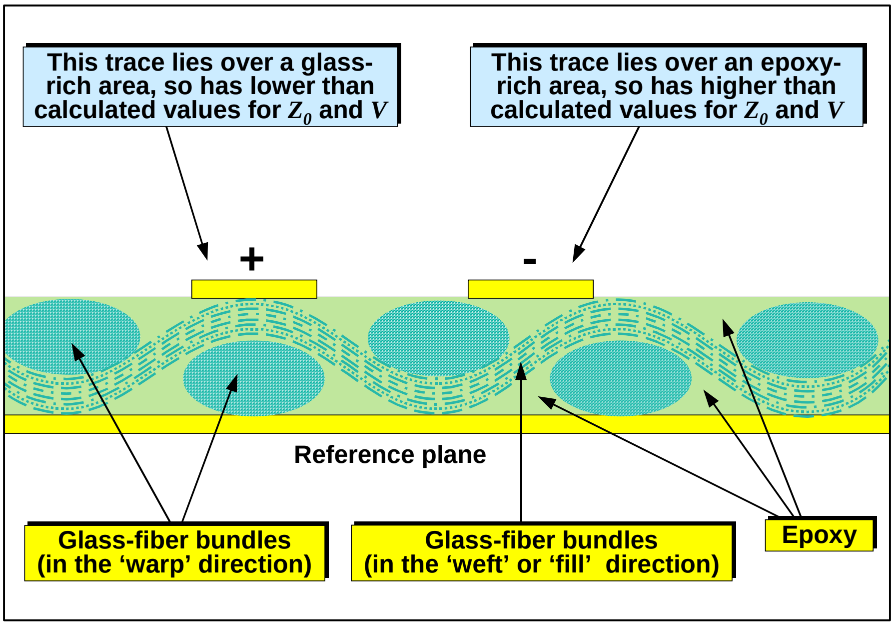



**Fig. 9 Glass fibres affect trace velocity and cause differential skew**

A current method is shown in Figure 10. It uses just one or two layers of a homogenous dielectric in a stack-up that is predominantly FR4 or a similar woven glass-fibre material. The stack-up is designed so that it is the homogenous layer(s) that govern the $Z_0$ and $V$ of the differential pairs [15] [16]. Not all PCB manufacturers are able to laminate such PCBs. Before committing to a manufacturer, accelerated life testing is recommended to prove that, over the lifecycle of the product with all its temperature fluctuations, their PCBs will not delaminate.

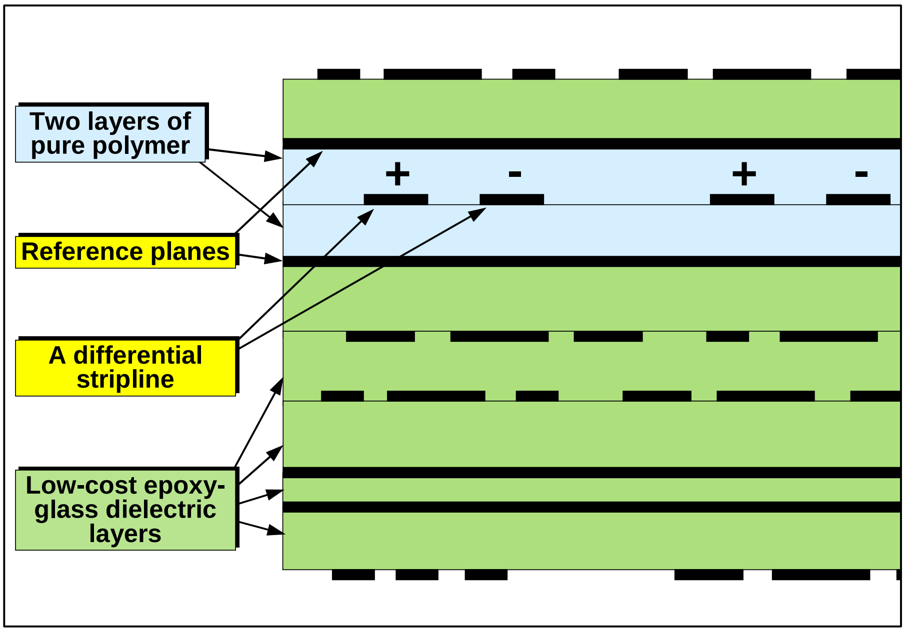



**Fig. 10 A stack-up that combines homogenous and glass-fibre dielectrics**

### Microstrip imbalances due to coatings

Solder resists, component legends ('silk screens'), conformal coatings or encapsulation can all be applied to the outer layers of PCBs, where they have an effect on any microstrip lines. The dielectric constants and loss factors of these materials are often not well characterized, and their coating thicknesses are often not very well controlled and PCB manufacturers are often allowed to use alternatives. So these coatings can cause variations in the $Z_0$ and $V$ characteristics of microstrips between different PCBs of the same design, and possibly cause variations over the width or length of a given board. Partial application of a coating can also cause imbalance in a trace pair.

One way of overcoming this is to ensure there are no coatings or printed legends over microstrip transmission line traces. Another is to include a number of test traces [8] at widely spaced locations on the PCBs and test them against specific performance targets at Goods Receiving before accepting any batch of PCBs. It will also help to specify the coating materials to be used by their manufacturers' part numbers.

Accidental coatings, such as condensation, liquid sprays and dust can also cause $Z_0$ and $V$ variations and imbalances in differential pairs. The dielectric constant of water is very high (around 80), and the deposition of condensation, spray and dust can be uneven, so these can be very important causes of imbalance.

For the above reasons, striplines are generally preferred for EMC where the layer changes can be controlled adequately as discussed above.

**Conclusions**

Differential transmission lines on PCBs suffer from a number of causes of imbalance, which can degrade their SI and EMC performance. This paper has briefly described the major issues, as well as some design techniques that can reduce their influences.

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