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# Part 7, Routing, Layer stacking, Microvias

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# Advanced PCB Design and Layout for EMC Part 7 - Routing and layer stacking, including microvia technology

**By Keith Armstrong C.Eng MIEE MIEEE**

This is the seventh in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm chip processes, 'chip scale' packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. **Routing and layer stacking, including microvia technology**
8. A number of miscellaneous final issues

A previous series by the same author in the EMC & Compliance Journal in 1999 "Design Techniques for EMC" [1] included a section on PCB design and layout ("*Part 5 - PCB Design and Layout*", October 1999, pages 5 - 17), but only set out to cover the most basic PCB techniques for EMC - the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC. Like the above articles, this series will not spend much time analysing why these techniques work, it will focus on describing their practical applications and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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## 1 Routing and layer stacking techniques, and microvia technology

This part of the series is concerned with the business of routing the traces on the PCB artwork, etching and plating the copper foils, laminating the etched foils with layers of dielectric, and drilling and plating the via holes. All of these can have an effect on a PCB's EMC.

Some of the relevant issues have already been discussed in previous parts of this series, in which case they will only be briefly mentioned here, with a reference to the earlier part. If you have missed any parts of this series, you can download them from the archive at http://www.compliance-club.com/keith_armstrong.asp or http://www.compliance-club.com/KeithArmstrongPortfolio.

But please note that the last two issues of the EMC & Compliance Journal are posted in full at http://www.compliance-club.com and articles are only placed in the archives when they are not in one of these - so if the part you want is the one previous to this, it might not yet have been transferred to the Journal's archives.

## 2 Routing

Previous parts of this series have described a number of PCB component placement and routing techniques, for example -

a) Part 2 [6] discusses the segregation (partitioning) of components and their associated traces into different zones, and how to route the traces that must interconnect the zones. It also covers component placement and trace routing in filter zones, and when shielding cans are used on the PCB.

b) Part 4 [7] discusses the design of planes, and the routing of traces with respect to plane edges, and also with respect to any splits or gaps in a plane.

c) Part 5 [8] discusses routing techniques for decoupling capacitors (decaps).

d) Part 6 [9] discusses routing techniques for traces that carry high-speed or high-frequency signals or noises - especially its section 3.1 and figures 6T-6W. It contains a lot about controlling trace characteristic impedance and propagation velocity, and when transmission line techniques are not required this may be ignored. But note that for good PCB EMC performance, transmission line techniques are increasingly required to prevent unwanted noises from causing emissions or immunity problems.

Most of the analysis of trace routing in the literature is based on reducing emissions. But by applying the principle of reciprocity, we find that the trace routing guidance that results in least emissions from traces (e.g. section 3 in [9]) also improves a circuit's immunity to high-frequency noise present in its operating environment.

Matched transmission line techniques [9] are also an important technique for reducing emissions from traces (by reducing the amplitudes of the standing waves, making traces less effective as 'accidental antennas'). So this technique will also, by reciprocity, make traces less liable to pick up noise from their environment - helping improve the immunity of their circuits.

The above parts have covered everything I want to say about trace routing, except for how to design traces which need to carry transient or surge overcurrents and/or overvoltages, which are covered later on.

## 3 Stack-ups

The 'stack up' is the name given to the order of the various etched copper foil and dielectric layers that are laminated together under pressure and heat to make a PCB. Some of the earlier parts of this series have made recommendations that affect stack-ups, for example -

e) Part 2 [6] discusses the use of plane layers in a stack-up when using shielding cans, and when using filters.

f) Part 4 [7] discusses techniques for dealing with the cavity resonances between planes in a stack-up, and what to do when traces must change layers along their route.

g) Part 5 [8] discusses decoupling using adjacent pairs of 0V and power planes, and its extension into what is often called 'buried capacitance'.

h) Part 6 [9] discusses stack-up techniques suitable for traces with specified characteristic impedances, and also for any traces carrying high-speed signals or noises. As mentioned in section 2 above, the same techniques are useful for improving a circuit's immunity to radio frequency (RF) noise in the environment, by making its traces less effective 'accidental antennas'.

The above parts have covered all the details that I wanted to cover on stack-up design, except for the

benefits of closer trace-plane spacing, closer component-plane spacing, copper balancing, and how to put all the techniques together and decide on the number of layers and the spacings between those layers. These remaining issues are covered below.

### 3.1 The benefits of closer trace-plane spacing

The EMC benefits of closer 0V-power plane pair spacing were described in [8], but there are also EMC benefits from having closer spacing between *traces* and planes. A significant cause of PCB emissions is the conversion of the wanted differential-mode (DM) signals into unwanted common-mode (CM) noise. The CM noise is then radiated from traces, planes, attached cables and other conductors behaving as accidental antennas. Because of reciprocity, the reverse process (CM to DM conversion) is a significant cause of susceptibility. The resulting DM noise in the PCB traces interferes with circuit operation, either directly or via demodulation or intermodulation in semiconductors.

But when a trace's width becomes comparable with its spacing from a substantial plane, the CM-DM conversion ratio (and the DM-CM ratio) starts to reduce, improving emissions and immunity. Now, if the trace-plane spacing is halved, or the plane dimensions are doubled, the CM emissions generally reduce by about a half (approximately 6dB). Continuing to reduce trace-plane spacing, or increase plane dimensions, causes the CM emissions to continue to fall proportionately.

This is a most desirable situation, and since many traces on PCBs are now in the region of 0.25mm (10 thousands of an inch, called 'thou' in the UK and 'mil' in the USA) to 0.18mm (7 thou), we should now be aiming to use trace-plane spacings with the same dimensions, or less. Ideally, the trace-plane spacings should be half the trace width, and the planes as large as possible. It may even be worth making a PCB larger all around and filling the extra border space with 0V plane (and nothing else) to improve EMC. This would have the added benefit of reducing the fringing fields, improving the EMC performance of the PCB even more.

Traditional PCB stack-ups use equal layer spacings, for no good reason, so the idea these days is to use unequal layer spacings. Of course, if a PCB has so many layers that equal layer spacings results in trace-plane spacings of around 0.15mm (6 thou) or less (e.g. a 1.6mm thick PCB with ten or more layers) then equal layer spacings might be able to be used.

A possible problem with very small trace-plane spacings is their effect on characteristic impedances of traces, discussed in [9]. When using smaller trace-plane spacings it becomes more difficult to achieve higher values of $Z_0$ without using very fine-line PCB manufacture, which might cost more. For example, a microstrip using a 0.2mm (8 thou) trace in 1oz copper spaced 0.15mm (6 thou) from its plane would have a $Z_0$ of about 58Ω, and to achieve more than 80Ω would require a trace width of less than 0.1mm (4 thou) using «oz copper.

### 3.2 The benefits of closer component-plane spacing

Reducing the spacing between the semiconductors in the ICs and a copper plane in their PCB allows the image-plane effect (see section 1 of [7]) to reduce the emissions and improve the immunity of the devices themselves.

Also, decreasing component-to-plane spacing reduces the lengths of the via holes between an IC or decap and its 0V and power planes, and also reduces the area enclosed by the current loop created by the decap and the device it is decoupling. Both of these are beneficial for decoupling (see section 2.5 of [8]) especially when very low-inductance decoupling current loops are required for controlling the noises emitted by modern digital ICs.

### 3.3 Copper balancing

An inequality in the 'balance' of copper in a PCB about the centre-line of its stack-up (e.g. 0.8mm through the thickness of a 1.6mm PCB) can cause the PCB to warp when put through the high temperatures of an automated soldering machine, or during long use at elevated operating temperatures. A warped board is bad because it can cause solder joints to fail prematurely, and it can even pull the terminals off large surface-mounted devices or pull the pins out of large leaded devices.

With lead-free soldering about to happen on a large scale, it should also be realised that a warped board applies mechanical stresses to its soldered traces and devices and this encourages the growth of tin whiskers, with 1mm long conductive whiskers being possible in such circumstances. Such tin whiskers are also a possible cause of unreliability (and maybe safety hazards too, see section 7.2 below).

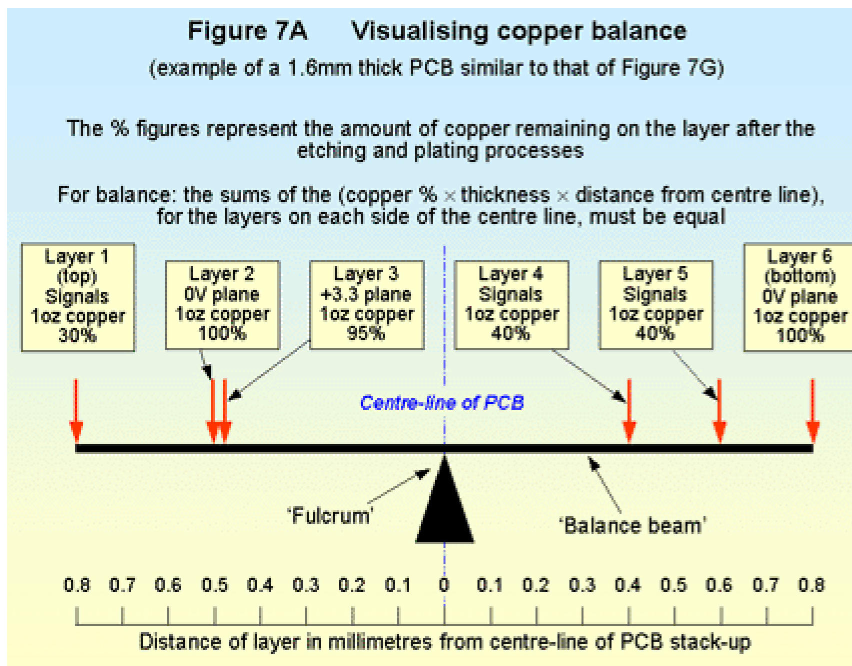
The copper balance of a PCB depends on the percentage of the copper left unetched on each layer (a solid plane over the whole area being 100%), the finished thickness of the copper foil (after etching and any plating), and the distance of each layer from the PCB's centre-line.

Calculating copper balance is like taking a balance beam with a central fulcrum and placing different weights at different distances from the fulcrum, so as to get the beam to lie horizontal (i.e. to be in balance). Some PCB stack-up management applications can calculate copper balance automatically, but it isn't too difficult to do by hand for PCBs up to eight layers by using the 'balance beam' analogy - because the maths is so simple to understand.

Copper balance has traditionally been achieved by using equally-spaced layers and a symmetrical PCB (symmetrical construction about its centre-line). A symmetrical PCB is one that has mirror-image stack-up either side of its centre line, for example the following equally-spaced stack-up:

Layer 1 Signal
Layer 2 Signal
Layer 3 Plane
*(Centre-line)*
Layer 4 Plane
Layer 5 Signal
Layer 6 Signal

The signal layers in the above example would need to have the same copper thicknesses, and the PCB designers will add hatched or filled copper areas that have no circuit function to maintain the same copper percentages and achieve uniformity over their areas. The plane layers would use the same copper thickness.




To avoid having to determine how much copper fill was required to make all of the signal layers have a similar unetched percentage, some companies use symmetrical stack-ups and automatically fill **all** of the areas that would have been etched with non-functional copper - on **all** of the signal layers. Then all of the layers (including planes) can be treated as having the same copper percentage, so that copper balance can then be achieved simply by using equal layer spacing and an even number of layers.

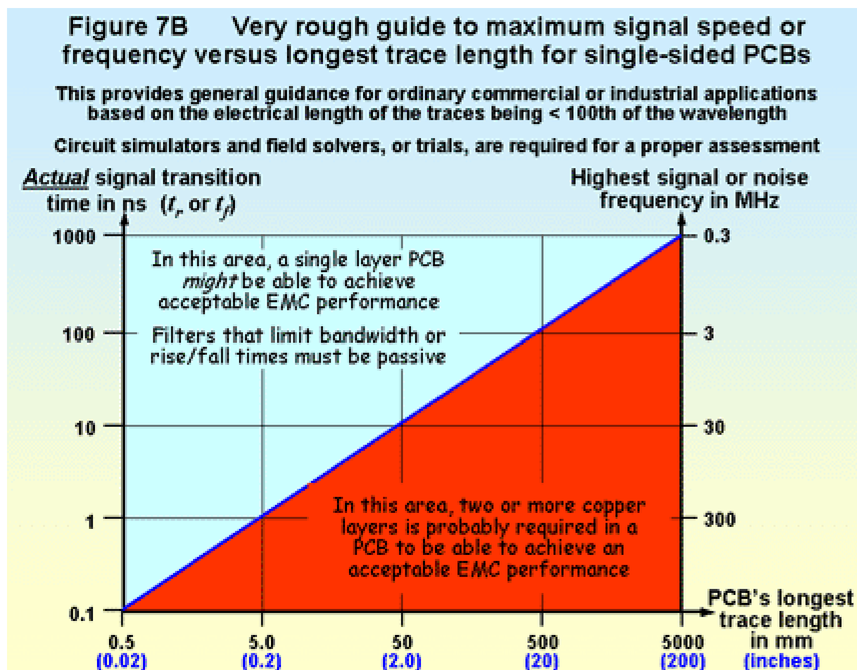
Unfortunately, the use of hatched or filled areas can have bad consequences for EMC, as discussed in section 4 below.

The above copper balance methods are simply ways to avoid doing any work, and perfectly good copper balance can be achieved using unsymmetrical layouts with different copper percentages, thicknesses, and unequal spacings, at the cost of a little extra design effort and time. This enables the use of closer trace-plane spacings (see 3.1 and 3.2 above) and also helps to avoid the EMC problems caused by hatched or filled areas (see later).

### 3.4 Single-layer PCBs

These types of PCBs provide very limited control of the EMC characteristics of their traces. So they should never be used where any degree of EMC performance is required, except for circuits specially designed by someone who understands how to choose the components and design the circuit to compensate for the 'accidental antenna' effects of the PCB traces. They can be acceptable where the signal bandwidths are limited by design by passive filters, to less than a frequency that depends on the size of the PCB.

Figure 7B shows some general guidance based on the wavelength of the signal or noise being larger than 100 times the length of the trace, which might be able to provide acceptable EMC performance in some general-purpose household, commercial or industrial applications. Field solvers and circuit simulators are required to predict EM performance with any reasonable accuracy (see section 4 of Part 1 of this series [10] for more on this). Of course the good old fashioned method of designing, testing and redesigning can be used instead - if there is plenty of cash and time available - or if the design is being done by an EMC circuit and PCB design expert.




Note that all semiconductors (except for the very largest power devices) will respond quite happily to frequencies in excess of 100MHz, either by direct interference with the wanted signal or by demodulating or intermodulating them to cause interference at other frequencies from d.c. upwards. Even very low-cost operational amplifiers with gain-bandwidth products of 1MHz or less and slew rates of 1V/µs or less will happily demodulate at well over 1GHz. So only passive filters may be used to limit the bandwidths or rise/fall times of the signals in the traces of single-layer PCBs. (Note that a feedback capacitor from output to inverting input on an opamp is an *active* filter, and not suitable for any EMC purposes above 1MHz or so, depending on the opamp.)

Modern sub-micron digital ICs and RF devices are generally unsuitable for use on single-layer PCBs.

### 3.5 Two-layer PCBs

Two-layer PCBs can provide much better control of the accidental antennas that we call traces, if carefully designed. But it is very hard to make them achieve acceptable EMC performance when using modern digital devices with their very short rise/fall times.

Sections 2.3 and 2.7 of [7] discuss how to make a two-layer PCB achieve the best EMC performance they are capable of, preferably by using the 'solder side' layer as a solid 0V plane, or at least by creating a 0V mesh by creating a 0V fill on both sides of the PCB and 'stitching' them together with vias. And section 2.7 of [8] describes a ferrite decoupling technique that can be very effective on two-layer boards. These techniques will not be described again here.

As for single-layer PCBs, only passive filters may be used to limit the bandwidths or rise/fall times of the signals in the traces to make the EMC performance acceptable.

RF and microwave designers have traditionally used two-layer PCBs and had excellent EMC performance, but one side was always a solid plane and the single signal layer always used well-matched transmission lines. So it is also possible that modern sub-micron digital devices could achieve good EMC performance using two-layer PCBs by using the same techniques - but only if they could fit all of their signal routing into the one signal layer available.

So sub-micron digital ICs and RF devices are not generally suitable for use on two-layer PCBs.

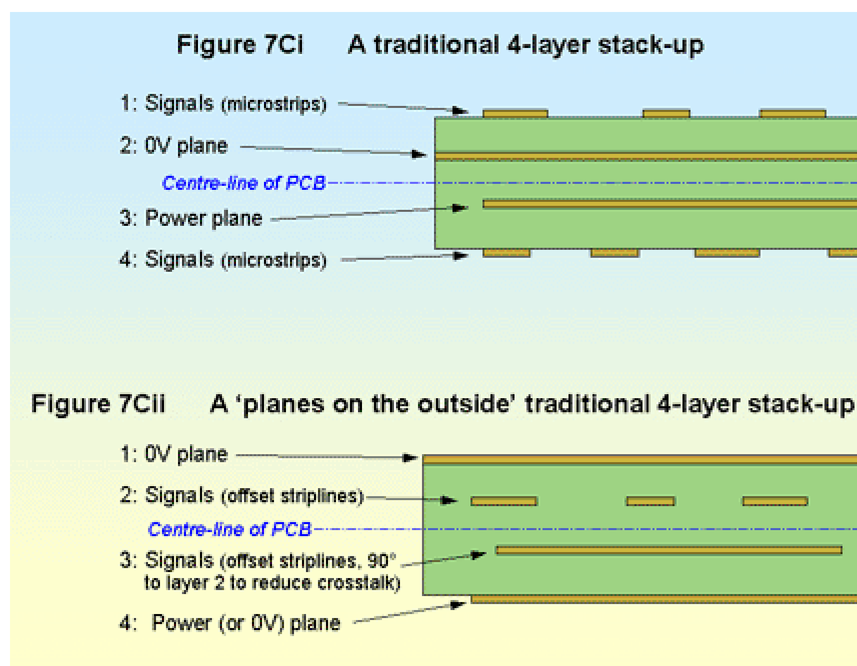
However, there are a small number of modern microcontrollers that claim to have been designed with EMC in mind for use in very low-cost products (e.g. for the automotive industry), such as the Fujitsu F$^2$MC-16LX family, and these may be able to be used without matched transmission lines, and without solid 0V planes so that they can be fully routed can be achieved on a two-layer PCBs.

As for single-layer PCBs, field solvers and circuit simulators are required to predict the EM performance of two-layer PCBs with any reasonable accuracy (see section 4 of [10]). Of course the good old fashioned method of designing, testing and redesigning can be used instead - if there is plenty of cash and time available - or if the design is being done by an EMC circuit and PCB design expert.

### 3.6 Four-layer PCB stack-ups

The state-of-the-art for the majority of commercial products during the 1980s, and still capable of providing adequate EMC performance throughout much of the1990s - the four-layer PCB can still provide adequate EMC performance (if carefully designed) with digital devices based on IC design rules *at least* one generation larger than 150µm.

Figure 7Ci shows a typical equally-spaced four-layer PCB stack-up of the 1980s, which obtains some decoupling benefits from the distributed capacitance of its embedded 0V/Power plane pair.




Some designers prefer to place the two planes on the outer layers, and reserve the inner layers for signal traces, as shown in Figure 7Cii. The idea is to shield the traces, but even with a via or decap wall around the PCB's perimeter [8] (which is not usually incorporated) the plane on the component side would be badly perforated by the pads and pin-escapes for the devices, and so incapable of providing high levels of shielding.

Some useful shielding might be achieved with careful design (and a via or decap wall) but this must be balanced against the fact that when using a 0V and a power plane - they are so far apart that they no longer provide any appreciable decoupling benefits from their distributed capacitance. Whether the result would be better than the stack-up with the embedded planes would need a circuit simulator combined with a field solver to predict.

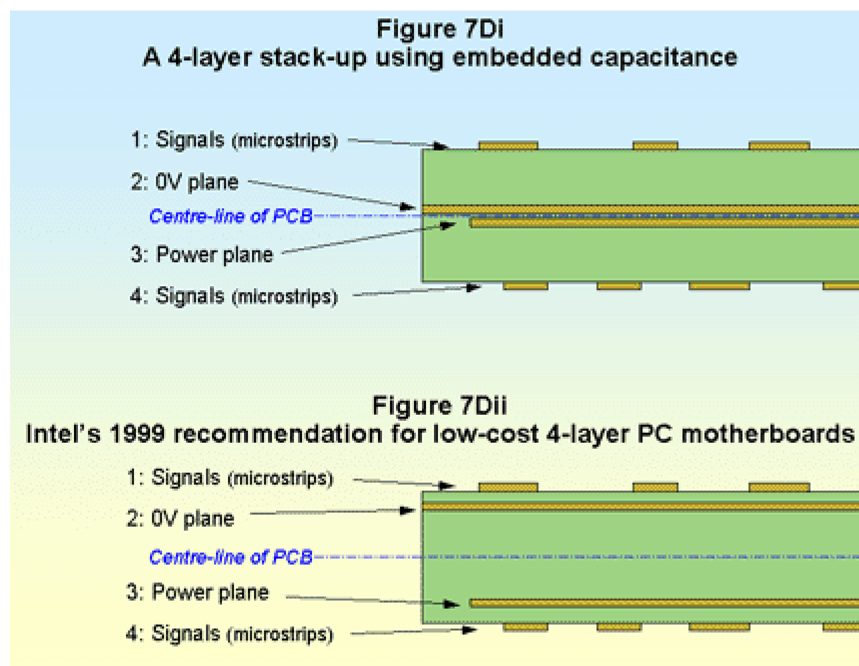
Another issue with this 'planes on the outside' stack-up is that it is very difficult indeed to hand-

modify traces on prototype PCBs during development. Some companies would make all their prototype PCBs using an embedded pair of planes, changing to external planes for the production version once all the development was (hopefully!) complete. Of course, this stack-up change could make a significant change to the EMC performance of the PCB, and alter the characteristic impedances of the traces, making the assumption of "no further changes required" more risky.

The traditional stack-ups shown in Figures 7Ci and 7Cii are both symmetrical, and both use equally spaced layers.

Figure 7Di shows a stack-up using unequal layer spacing to try to improve decoupling through the use of embedded capacitance. The 0V/power plane pair must be aligned on the centre-line of the PCB otherwise it is impossible to achieve copper balance and board warp can occur - but the problem is that the outer (signal) layers are now so far away from their reference planes that their EMC characteristics are not so good.

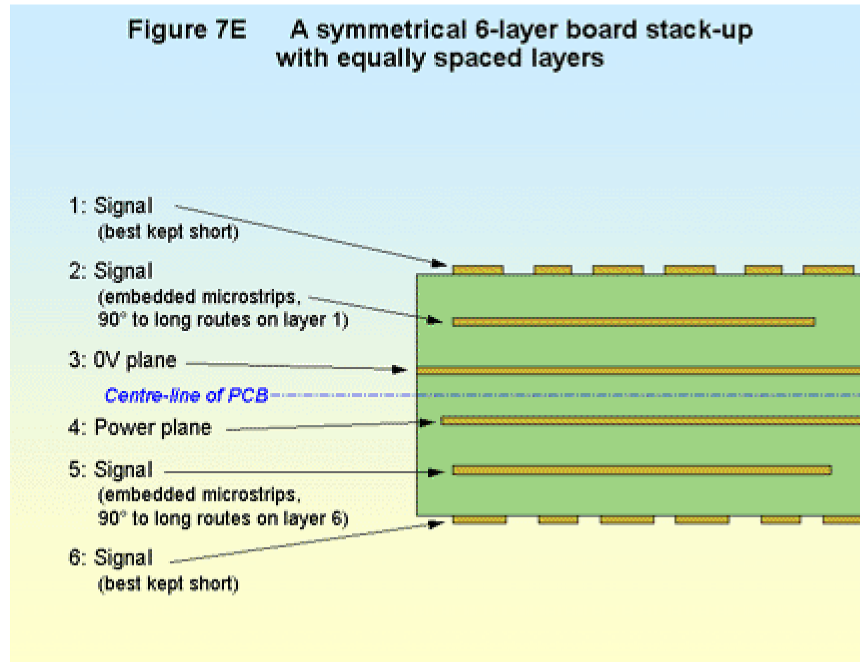
Figure 7Dii shows a stack-up recommended by Intel for low-cost PC motherboards in the late 1990s, which also has a symmetrical stack-up but uses unequal layer spacings to reduce the trace-plane spacings for the outer signal layers, so they can handle high-speed digital signals with better signal integrity (SI). This stack-up is suitable for mounting 1990s technology digital ICs and their high-speed traces on both sides, but the 0V and power planes are so far apart that their distributed capacitance provides little benefit for decoupling. Good SI and good EMC performance are closely related, as discussed in section 1.2 of [9] and [11].



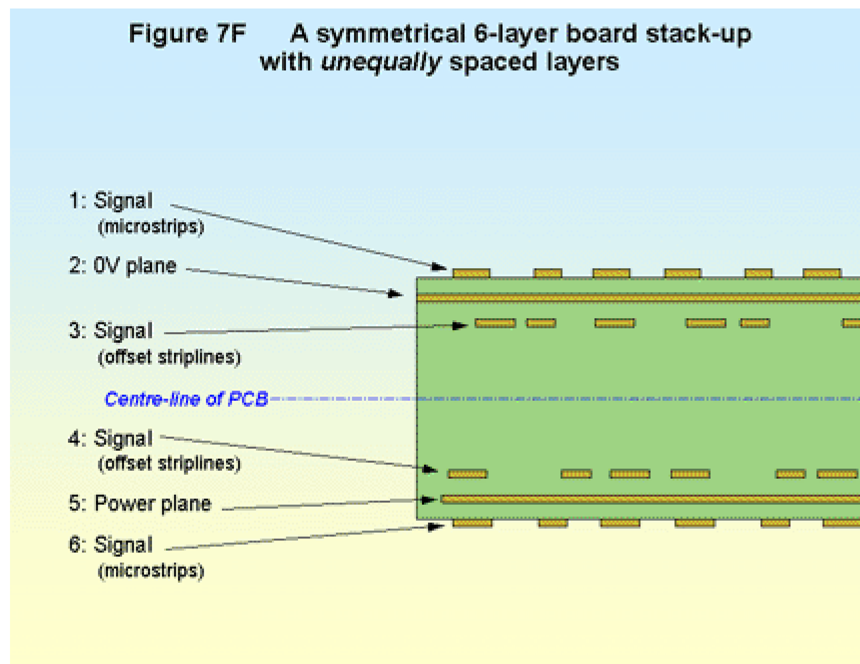

It is worth noting that the typical desktop or tower PC cases in the late 1990s achieved a shielding effectiveness of about 50dB at 30MHz falling to between 15 and 35dB at 1GHz, so this four layer construction would probably not have complied with FCC or EU EMC regulations without such a shielded enclosure. It is also worth noting that high-performance servers and workstations based on PC technology in the late 1990s would have used PCBs with eight or more layers, and shielded cases. (And some people have reported them as experiencing lower levels of 'Windows crashes' even when running the same operating systems and applications software, so maybe the SI of the four-layer boards was not the best).

### 3.7 Six layer PCBs

A six-layer PCB gives more design flexibility than a four-layer, but it takes some work to make it ideal in EMC terms. Figure 7E shows a traditional symmetrical stack-up with equally-spaced layers, which has no EMC advantages over the equivalent 4-layer PCB - it just has two more layers for signal routing.



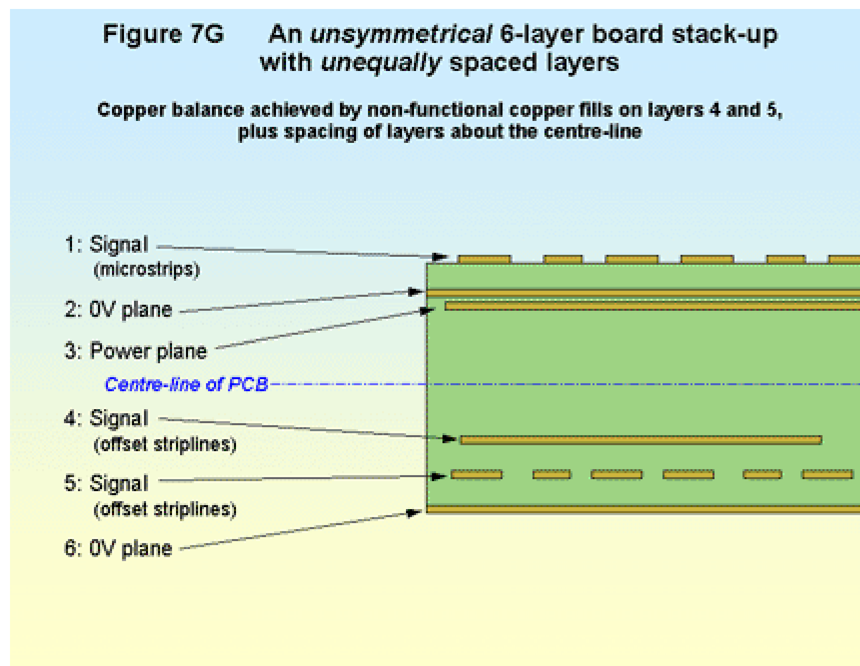

Using an unequally-spaced stack-up as shown in Figure 7F has the EMC and SI advantages of the Intel recommended design shown in Figure 7Dii, with the advantage of two internal offset stripline layers. To maximise the EMC potential of this stack-up, the traces on the outer layers should be kept short and all high-speed signals or noises routed on the inner signal layers. Unfortunately, like Figure 7Dii, this stack-up has very little distributed capacitance between its 0V and power planes.




Using an *unsymmetrical* stack-up with unequally-spaced layers as shown in Figure 7G can improve the EMC of the previous design (Figure 7F), at the cost of one less signal routing layer and more effort required to achieve a copper balance. The 0V and power plane pair are placed very close together to maximise their distributed capacitance, and they are located close to layer 1 so that

devices mounted on this side have less decoupling inductance (see 3.2 above). The bottom layer has been made a 0V plane so as to retain the two offset striplines.

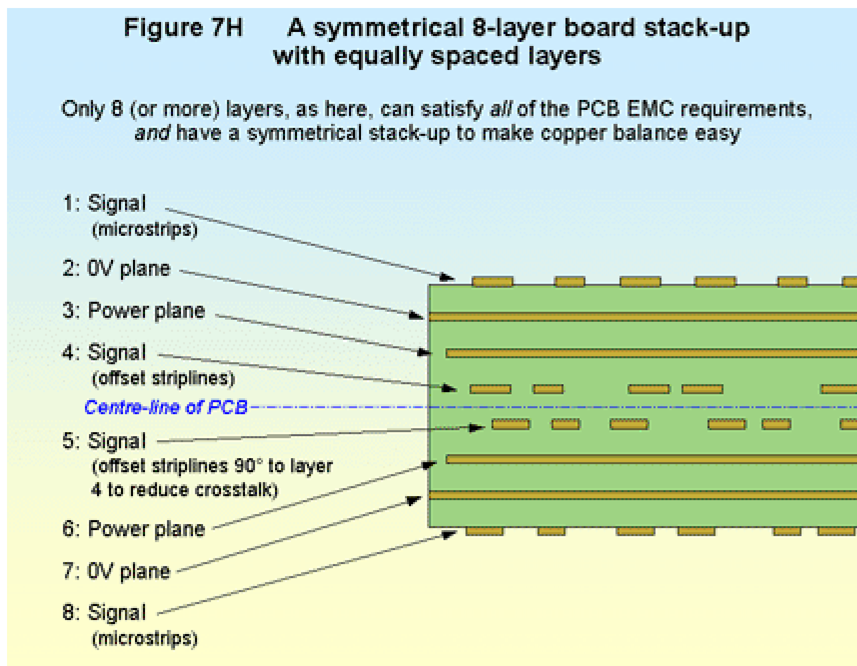
This stack-up is best when used with components mounted on its top side only (the layer 1 side), or with double-sided assembly where the bottom side is used for passives or slower devices and/or signals. Note that the decaps for the ICs on the top side, should also be mounted on the top side, to minimise decoupling inductance.



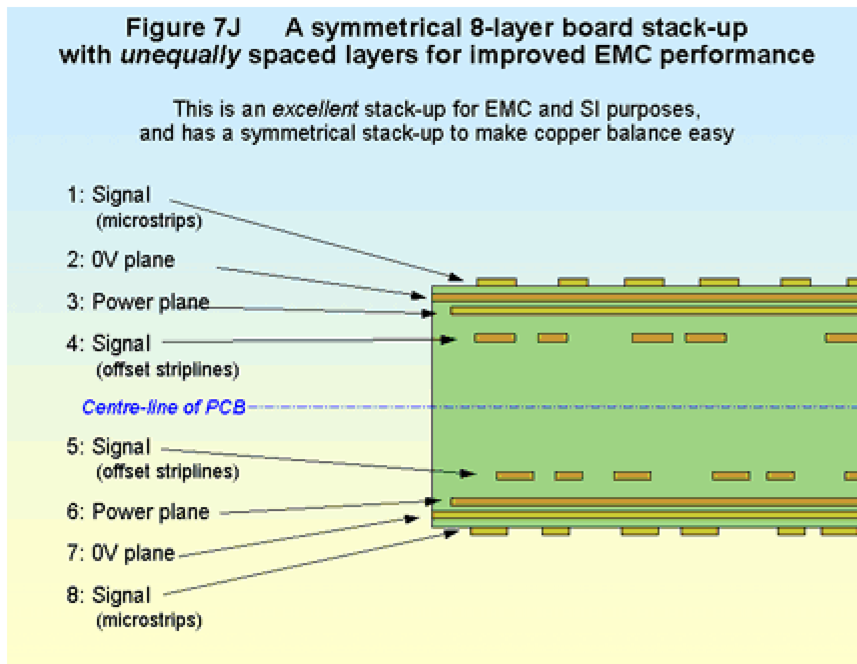

### 3.8 Eight layer PCBs

The eight-layer PCB is the only symmetrical stack-up that can meet all of the EMC requirements for a stack-up without requiring a lot of design effort. It will also support fast devices on both sides, which six-layer stack-ups with equivalent EMC performance (e.g. Figure 7G) cannot do.

Figure 7H shows a traditional design using equal layer spacings, with four signal layers and two pairs of 0V/power plane pairs. The best routes for traces carrying high-speed or high-frequency signals or noises is on layers 4 or 5, the offset striplines, so traces carrying all such signals or noises on layers 1 or 8 should be kept as short as practical.




If the PCB is 1.6mm (64 thou) thick, the spacings between the layers might be small enough (0.23mm, 9 thou) to achieve enough improvement due to closer trace-plane spacing, significant distributed capacitance, and low decoupling inductance. But significant improvements are possible by using unequal layer spacings whilst retaining the symmetrical stack-up (which makes design very easy) and an example is shown in Figure 7J.




The stack-up shown in Figure 7J can be made optimal for EMC and SI, and is highly recommended as the starting point for all designs that use modern digital devices.

### 3.9 PCBs with more than eight layers

The eight layer design shown in Figure 7J (symmetrical, with unequal layer spacings) can be designed to be optimal for EMC and SI, and adding extra layers does not add any extra EMC benefits.

The two closely-spaced 0V/power plane pairs, each spaced very close to the outer layers to aid decoupling, can provide all the decoupling that is required (apart from bulk capacitance) if they are made into real embedded capacitors by the use of high-k dielectrics and/or very close plane spacings (see section 3.14 of [8]).

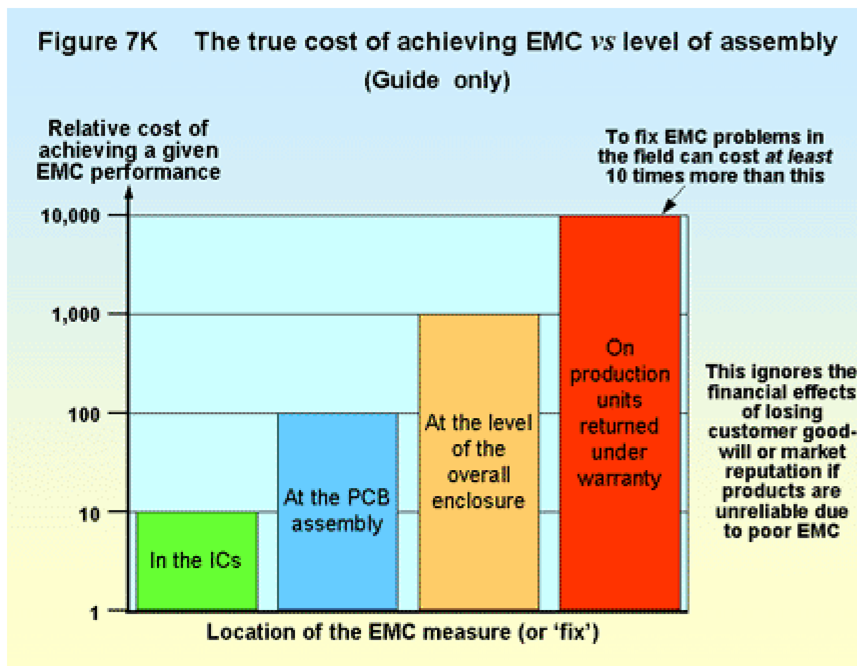
So extra layers are simply a routing issue, and they can all be signal layers with additional 0V planes as required, to help control trace characteristic impedance and crosstalk. These extra layers should fit between layers 3 and 6 on Figure 7J, so as not to upset the excellent decoupling provided by the 0V/power plane pairs for the ICs soldered to the top and bottom layers of the PCB.

### 3.10 Number of PCB layers and cost-effective design in real-life

More than 50% or the world's production of PCBs now use 6 or more layers, and they are used in personal computers and cellphones that cost much less than equivalent products - using simpler PCB technologies - did years ago. So when anyone complains about the cost of extra PCB layers, or of the use of more modern PCB technologies (e.g. HDI, see later) - they should generally be sent for re-training.

I recently used an eight-layer stack-up similar to the one shown in Figure 7J to reduce emissions in the 700-900MHz range by over 20dB, for a PCB that originally had six layers. The manufacturer had laboured for over 9 months to try to reduce these emissions to achieve EMC compliance, using filters, shielding, etc. - but simply replacing the PCB with the eight-layer version was sufficient on its own to create the required improvement. The extra cost of the 'bare board' turned out to be minimal, especially when compared with the extra costs that the les effective filtering and shielding would have required.

It is often the case that designers don't consider increasing the number of layers in a PCB because of the intense pressure on 'BOM cost' from their managers (BOM = bill of materials). But, as explained at some length in Part 1 of this series [10], it generally makes the very best economic sense to solve EMC problems at the lowest level of assembly, and after the ICs themselves, this means solving them at the level of the bare PCB. Even if the bare board costs more in volume manufacture, due to additional layers, the real-life cost saving from a correct PCB EMC design will generally be at least ten times the bare board's extra cost. The profitable selling price of a product is **not** determined by simply multiplying the cost of its BOM by some pre-determined number (see section 1.2 of [10] for more on this). This issue is so important that Figure 1B from [10] is repeated here as Figure 7K.




When a company is using six or fewer layers in their PCBs and a designer is considering adding extra PCB layers for EMC or SI reasons, the designer generally asks his company's buyer to get a quotation for the bare board. The resulting quotation is often as much as double the price of the existing board, which frightens off the project manager (even though it may still be very cost-effective in real-life) because most of them treat the lowest BOM cost as some sort of holy quest.

But it is important to realise that except for PCB manufacturers that specialise in low-volume work, all PCB manufacturers specialise in the number of PCB layers they aim to make most cost-effectively. So the PCB manufacturing plants are optimised for single-sided, double-sided, four-layer, or six-or-more layers. Each plant will only be able to give the best quotation for PCBs with the number of layers that their machines and processes are optimised for.

So now we can see why the request to the company buyer came back with such a high price for the extra layers - the buyer simply asked his existing PCB suppliers. To get the correct price for a PCB with added layers generally means discovering **new** PCB manufacturers whose plants are optimised for that number of layers, and asking them for a price. For example, in high volumes a bare four-layer PCB typically costs up to 25% more than a double-sided board that is otherwise identical. But most buyers do not know this, so make sure to tell them.

Adding 0V and power planes and thereby increasing the number of layers in a PCB is one of the most cost-effective EMC measures available, yet it is often ignored or denied due to buyers' lack of knowledge of PCB manufacturing, and project managers' short-sighted focus on BOM costs and lack of understanding of the real-life costs associated with manufacturing a product.

### 3.11 Shielding power planes with different voltages

Where power planes with different voltages are parallel to each other in a stack-up, they will couple noise from one into the other. This can cause high-frequency noise (e.g. from a 1.2V plane associated with a high-speed processor core) to spread more widely around a PCB and hence cause SI and EMC problems. To reduce the noise coupling between different voltage planes, place a 0V plane between them. Of course, like all 0V planes it must connect to all the other 0V planes as described in [7].

## 4 EMC issues with copper balancing using area fills or cross-hatches

As mentioned earlier, a copper imbalance in a PCB can cause it to warp when put through the high temperatures of an automated soldering machine, or during long use at elevated ambient temperatures. This is bad because it can cause solder joints to fail prematurely. It can also encourage the growth of tin whiskers when using lead-free components and soldering - another cause of unreliability (if not safety hazards, see section 7.2 below).

Hatched or solid-filled copper areas, that are non-functional, are generally used to create a more uniform copper balance over the area of a PCB layer, and also used to increase the total unetched percentage of copper in a layer. These are usually called 'poured grounds' or 'ground fills', when they are connected to the 0V. Because planes are solid (mostly unetched) copper their copper percentage is close to 100%. Because it has been traditional to create symmetrical PCB stack-ups with equal layer spacings, in some companies the practise has arisen of automatically performing a copper fill on every layer so that they all have a similar overall percentage to that of the plane layers. Then copper balance is automatically achieved without anyone having to think about it.

Apart from the fact that any PCB design practices that are used without understanding and regular review are potentially **bad** practices - automatic copper fills can be bad for EMC.

One EMC problem is that the hatched or filled (poured) areas can resonate and increase emissions and/or worsen immunity. This can be solved by connecting each hatched or filled area directly to the PCB's solid 0V plane (or power plane) by *at least* one via every $\lambda/10$ - where $\lambda$ is the wavelength of the highest frequency of concern, taking the dielectric constant of the PCB's dielectric into account.

For example, if the highest frequency of concern is 1GHz, and the PCB is using FR4 dielectric (relative dielectric constant above 1MHz = 4.2), the $\lambda$ of the 1GHz signal or noise inside the PCB is 150mm, so the hatched, filled or poured copper areas should be via'd to a solid 0V plane *at least* every 15mm. More frequent 0V via connections will be better for EMC.

Sometimes the hatched or filled areas are intended to reduce crosstalk, but they will only do that effectively if they are via'd to the PCB's solid 0V plane as described above for EMC.

The other EMC problem with hatched and filled non-functional copper areas is their effect on the characteristic impedance of nearby traces - which can be bad for both SI and EMC. I've seen examples where traces travelled into PCB areas where there were more areas of copper fill nearby, and their $Z_0$ fell by about 30% as a result. In the case of differential traces, differing amounts of copper fill on each side causes imbalances in the line, which is also bad for SI and EMC (see figure 6AG of [9] and its associated text).

The copper hatching and filling is usually the very last thing to be done to the layout before being sent for manufacture, and sometimes it may not have been present on the layouts that were reviewed by the circuit designer, or tested in prototypes. The assumption seems to be that the copper hatching or fill has no electrical effects, it is just a device to prevent board warp - but this is very far from correct.

Howard Johnson says that he doesn't use copper fills at all in multi-layer boards [12]. But they can be used, if their EMC and SI effects are understood and accounted for.

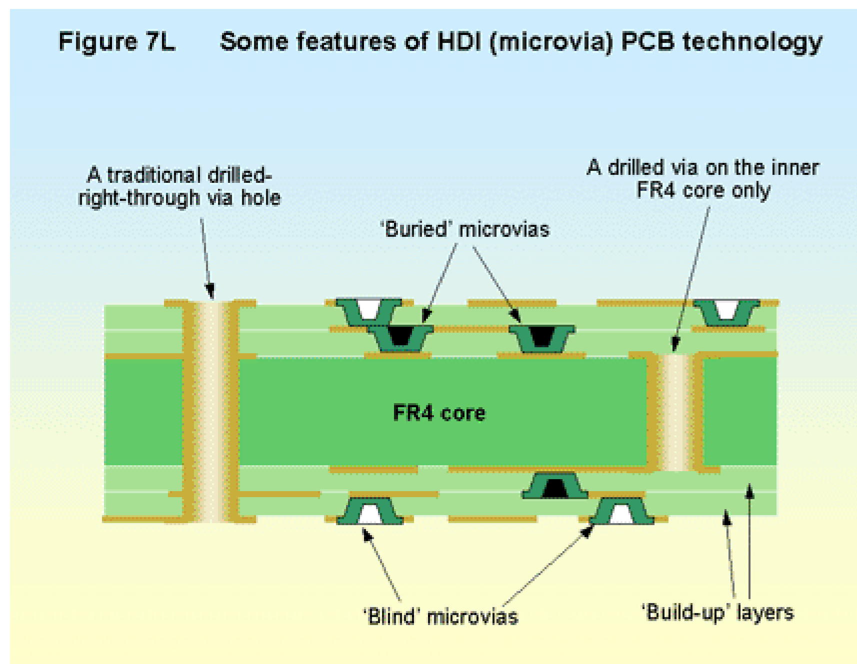
## 5 HDI PCB technology

### 5.1 What is HDI?

High Density Interconnect (HDI) PCB technology is also known as: 'microvia', 'sequential build-up' or simply 'build-up'. In this series I shall call it HDI, following [13]. It is based on the use of via holes of 6 thou (0.15mm) diameter or less, which can go between layers in a PCB without needing to

go through all of the layers. These are generally called 'microvias', and they can be 'buried' or 'blind'.

Microvias are created by drilling and through-plating the vias between each adjacent pair of copper layers separately, **before** they are laminated together to create the finished PCB. When the end result is a via that only connects between internal copper layers, it is called a buried microvia. When the result is a via that connects to one outer layer of the PCB and not to the other, it is called a blind microvia. Traditional drilled and plated all the way through the PCB vias can also be used along with buried and blind microvias. These basic features are shown in Figure 7L.




The way that microvias are created, they are always closed off at one end, so they don't 'steal' solder during reflow soldering. This allows via-in-pad layouts to be used, which saves PCB area and is very good for the PCB's decoupling performance, because it reduces the inductance of the decoupling current loop.

HDI techniques can reduce the area of PCB required by 40%, reduce the number of layers by 33%, and be much easier to design than through-hole-plated (THP) PCBs [14]. HDI techniques help to make the smallest, lightest, and least power-hungry products, and can be found in a wide variety of common products, such as cellphones and even some toys. Some high-reliability products use HDI because microvias are more robust than vias that are drilled and plated right through a PCB. A comprehensive review of HDI and its benefits can be found in [14], and the basic standard for the design of HDI PCBs is IPC-2315 [13].

### 5.2 The EMC benefits of HDI

These include…

- via-in-pad reduces decoupling inductance and increases decap resonant frequencies
- the shorter traces become efficient 'accidental antennas' at higher frequencies
- the shorter traces might not need to be treated as matched transmission lines
- the smaller PCBs resonate at higher frequencies
- HDI 0V planes aren't as heavily perforated as those of THP PCBs so they have lower impedances (hence lower PCB emissions and better immunity); they provide a more constant return path inductance for improved $Z_0$ control of transmission-line traces. They also achieve

more benefits from the image plane effect, and provide better shielding between the circuits on the top and bottom sides of a PCB (lower crosstalk).

The above are all very valuable for modern sub-micron ICs, especially where ball grid array (BGA) devices are used - when the use of THP PCB technology results in severe plane perforation under and around the device - exactly where good EMC and good SI require the *most*

HDI technology makes it easier to use modern small IC package styles, such as ...

- Miniature or Micro BGA
- DCA (direct chip attach)
- Flip-chip
- CSP (chip scale packaging)
- Tape Automated Bonding (TAB)

These small ICs, and the smaller PCBs they allow, can generally be made to have excellent SI and EMC because their thinner packages place them in closer proximity to the 0V plane in the PCB, so the image plane effect is more powerful. Also, the smaller bond wires and lead frames means they are less effective as accidental antennas at frequencies below their first resonance, and their first resonance is at a much higher frequency, so these devices tend to emit less from their bodies.

However, a problem with these very small devices is that they allow much higher switching edges and higher-frequency noises to be conducted into the PCB's power distribution and signal traces, which can worsen emissions considerably. But they can generally be made to have *better* EMC than the larger devices they replace, if all of the recommendations in this series of articles are followed.

**5.3 HDI suppliers and costs**

The usual complaint when HDI is mentioned is that the BOM will cost more, making the products uncompetitive, but this is hardly ever true these days, for two reasons.

The first reason is that HDI PCBs in reasonable quantities should now cost less than their THP equivalents. A survey by the IPC in May 2000 found that HDI PCBs could be purchased for the **same** bare-board price as a 'traditional' THP PCB. More recently, Happy Holden said in [14] that HDI PCBs should cost less than the THP PCB required to do the same job. Designing without using buried vias can help reduce HDI costs even more, and since HDI PCBs are smaller than THP and tend to consume less power - cost savings may be able to be made in other areas of the product, such as power supply or batteries, enclosure, etc.

The second reason is that is that focussing on the BOM cost instead of the real-life cost of manufacture is a commonplace economic error (this was discussed section 3.10 above).

I remember the same complaint about BOM costs being raised when double-sided PCBs were first proposed, then again when through-hole-plate (THP) was developed, then again when 4-layer THP PCBs were starting to become necessary, and yet again when 4 layers were no longer enough. The change to HDI from THP is no different. Where miniature BGAs with less than 1mm pitch, or when chip-scale, DCA, TAB or flip-chip devices are to be used - HDI is probably an *essential* technology for getting EMC-compliant products with low warranty costs to market quickly, and selling them at competitive prices.

**5.4 HDI PCD design issues**

HDI requires a different approach to PCB layout, and some PCB design techniques may not always be able to be used. There are now many PCB manufacturers using HDI (there were at least 62 in

May 2000) and because many of them developed their machines themselves, their manufacturing techniques can vary and may need different PCB layout techniques. So always ask the HDI PCB supplier you are thinking of using what PCB design rules and restrictions they require to be followed.

### 5.5 More information on HDI

Describing HDI PCB manufacturing technology and all of its ramifications is beyond the scope of this article. Useful and informative references include [13] - [29].

## 6 Current capacity of traces

### 6.1 Handling surge and transient currents

EMC is not only about radio frequencies, it is also about transients and surges. One of the issues that often arises is the ability of PCB traces to handle the transient and surge currents that flow in the various circuits or protection devices. When a conductor (wire or PCB trace) is required to handle a transient or surge current, we can use the following guide to calculate its maximum current.

$I = 290 \times CSA / \sqrt{t}$
Where…
I = current in amps
CSA = cross-sectional area of copper in sq. mm
$t$ = time (in seconds) to fusing (melting)

This guide is only valid for values of $t$ up to 5 seconds. When the duration of the overcurrent is longer than 1 second, thermal convection and conduction effects start to become significant. These increase the current rating for the same temperature rise, but require a very much more complex equation.

Note that 1/2oz (finished) copper foil has a thickness of 17.5µm, 1oz copper 35µm, 2oz copper 70µm and 3oz copper 105µm. Multiplying the finished thickness of the copper foil by the trace width gives us its copper cross-sectional area (CSA), which can then be used in the above equation.

For example, a trace that is 0.18mm (7 thousandths of an inch) wide in 1oz (finished) copper (35µm), subjected to a rectangular current surge lasting 40µs, would have a maximum transient or surge current (before melting) of around 290A. The normal 'double exponential' unidirectional surge test waveforms used (e.g. in IEC 61000-4-5) specify their decay time at the 50% point - doubling this time approximates to a rectangular surge waveform with equivalent heating effect.

Underwriters Laboratories (UL) carried out some tests of their own [30], resulting in some guidance on the maximum current handling that would not result in an open-circuited trace. The guidance given by figures 7 and 8 in [30] seems to correspond pretty well with the above formula (but note that the horizontal axes of the graphs in its figures 7 and 8 say they are trace thickness, when in fact they are trace width).

But the above only considers the copper's transient or surge current carrying capacity. Copper can get very hot indeed before it starts to melt, and such high temperatures will damage wire insulation and PCB dielectrics, possibly causing delamination with consequent reliability problems.

Some suppliers publish transient current data for wires, typically for current surges with a 1s duration. A typical 1s rating for wire with a 0.5mm2 CSA and standard PVC insulation, with a normal operating temperature of 25øC, is 55A. This current will not raise the copper temperature above the standard PVC insulation's 160øC short-term temperature rating (standard PVC is rated

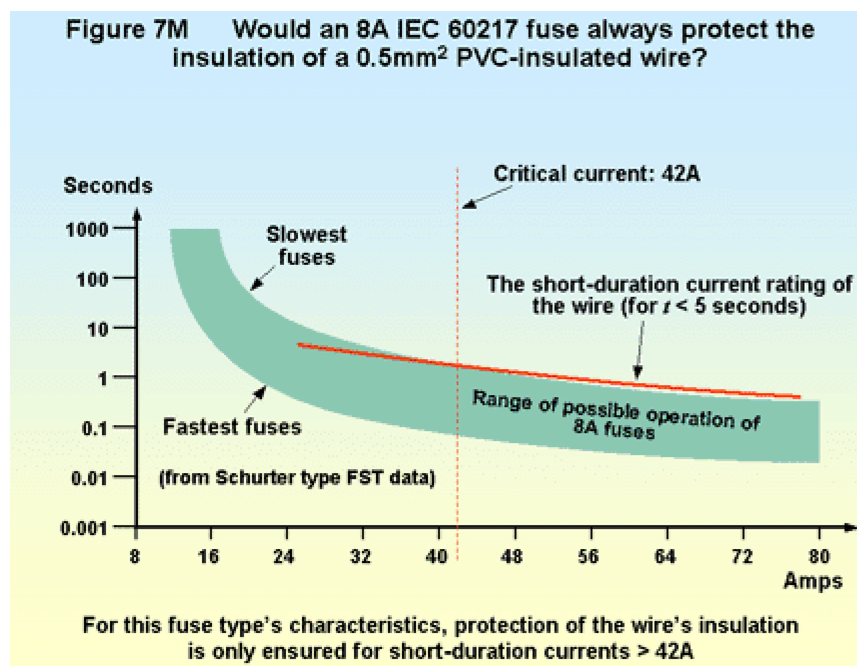
70øC for continuous use).

The transient current rating (for $t < 5$s) is proportional to the conductor's CSA and inversely proportional to the square root of the duration, i.e. the current rating for duration $t$ = (1s rating) $/\sqrt{t}$ .

In the absence of suitable guidance for PCBs we might choose the same guidance for PCBs made of FR4 and similar materials, since their continuous and maximum operating temperatures are similar to those of PVC.

Applying this guide to our example trace above - 0.18mm (7 thou) wide in 1oz (finished) copper (35µm), subjected to a rectangular current surge lasting 40µs - we find that when the normal operating temperature is 25°C it suggests that repetitive transient or surge currents of up to 100A should not cause damage to an FR4 PCB. Of course, this assumes that the transients or surges occur at a rate that allows the trace to cool down to 25°C after each one.

To protect a trace or PCB from an overcurrent that exceeds the values given by the above guides, we might want to use a fuse. But even the fastest fuses cannot respond in less than 10ms (which is a very slow transient or surge in EMC terms), and all fuses have tolerances on their operating speeds so it is important to design for the slowest one of the chosen type that might be fitted, as shown by the example in Figure 7M (which is for a wire and not a PCB trace, but the principle remains the same).




The melting temperature of copper is so high that any operating temperature up to 100°C would have little effect on the melting current rating. But the same is not true when we want to know the maximum current that will not damage plastic insulation or PCB dielectric.

When calculating the maximum permissible current for normal operating temperatures above 25°C, remember that the current allowed when the trace is at the maximum temperature of the insulation (e.g. 160°C) is zero, and that the heating effect of a current is proportional to the square of its value in Amps. So, in the above example, if the operating temperature was 60°C instead of 25°C, the maximum current that could be permitted before the trace temperature exceeded 160°C would fall from around 100A to around 86A.

High-temperature grades of FR4 and other dielectrics are available, and using them would allow

traces to carry higher transient or surge currents than the above guide suggests. On the other hand, some types of PCB dielectrics have lower short-term temperature ratings than FR4, so they would require lower transient or surge currents than the above guide if they are not to be damaged by hot traces.

It is best to use 'UL Recognised' or 'UL Approved' PCB materials, especially to prevent safety hazards from fire, smoke and toxic fumes, so always obtain and check the UL Approval certificate for the basic PCB material used (or other evidence). Some suppliers don't always deliver what they said they would, so check that all delivered PCBs have the appropriate UL logo stamped all over them.

### 6.2 Maximum continuous d.c. and low frequency current handling

Like surge and transient current handling discussed above, the continuous current handling of PCB traces is far from being an exact science. MIL-STD-275 [31] and IPC-2221 [32] are the published guides most often referenced for the continuous current capacity of a trace versus its temperature rise, trace width; PCB structure; ambient temperature; etc., but they are now considered inaccurate and incomplete [33]. The IPC has a project underway to create a new set of guidelines in IPC-2152 [33] [34], but it is not yet published.

John R Barnes provides guidance on PCB trace 'ampacity' on pages 31-87 to 31-92 of his excellent reference book [35]. Other useful references are [36] [37] [38] and [39]. This issue is not discussed further here; see the references below for how to deal with them.

### 6.3 Voltage drops in the PCB's power distribution

The voltage drop created as the d.c. current flows in the resistance of the power distribution system on a PCB (often called the IR drop) is also an important consideration in the design of a PCB. If a chip is operated on lower than nominal voltages, its noise performance can suffer and this can cause problems for EMC immunity and SI.

[40] says that for modern high-current low-voltage designs, it is becoming critically important to include package and board IR drop into the total noise budget of the system. This issue is not discussed further here.

### 6.4 Handling continuous RF currents

The traces associated with filters may have to cope with continuous levels of RF currents, with consequent heating effects. RF currents travel near the surfaces of conductors, due to the skin effect. The higher the frequency, the thinner is the thickness of the copper that is carrying the current. So as frequency increases the effective CSA of the copper decreases and the resistance increases, leading to a greater heating effect for a given RF current at a particular frequency.

Because they are continuous currents, the heating is dominated by conduction and convection losses (e.g. stripline gets hotter than microstrip (all else being the same) because microstrip benefits more from air convection). The proximity of a 0V or power plane in the PCB can make a big difference to the heat lost from a trace. So it is very complicated to calculate the maximum current of a PCB trace at a given RF frequency.

However, we can use the continuous d.c. rating of a trace (section 6.2) as a guide. If the skin depth at the frequency concerned exceeds the thickness of the copper trace, the d.c. current rating applies. But if the skin depth is less than the trace thickness, it is probably best to assume that the trace is only as thick as one skin depth.

The skin depth in plain copper is given by $d = 66/\sqrt{f}$ ($d$ in µm, $f$ in MHz), for example: at 160MHz $d$ = 5µm, (much less than the thickness of 1oz copper at 35µm) - so we would apply the d.c. calculations above assuming a copper trace thickness of 5µm, to calculate the temperature rise for a given current at 160MHz, or to calculate the maximum trace current at 160MHz.

### 6.5 A note on accuracy

Do not expect the above guides on current handling to be very accurate! It is probably best to limit the maximum currents to no more than 50% than they indicate, preferably less. When this current is not enough and a ’calibrated’ simulator is not available, it is best to make a ’test PCB’ with a representative trace structure and test and modify it until satisfied. EMC laboratories will be happy to provide surge or continuous RF test facilities. The test PCB should be made and tested very early in a project, to reduce project risks.

Where transient or surge currents lasting less than 1 second are concerned, heat conduction and convection are insignificant so the test PCB could consist of a single trace on the surface of the PCB. But this test PCB should use the correct copper thickness and trace width, and have a length similar to the final trace. Connecting the high currents to the trace needs to be done carefully to avoid problems at those points, so the trace should fatten to at least twenty times its width at both of its ends, and these wide ends soldered directly to connectors that suit the type of lead used by the transient or surge generator.

Where continuous currents are concerned heat conduction and convection are very significant, so the test PCB needs to have the correct structure (trace thickness, width and length; stack-up and dielectrics; spacing of all 0V or power planes, or embedded heatsinks; etc.), and the airflow and PCB operating temperature needs to simulate what is expected in the final product. The tested trace should have a similar shape (e.g. duplicating any sharp bends) but the layouts of the untested traces themselves don’t need to have any resemblance to the final PCB.

## 7 Transient and surge voltage capacity of layouts

### 7.1 Trace-trace and trace-metal spacing

The spacing between traces must be sufficient to handle the high voltages that arise due to transient and surge events. There is useful information on this in [30], but the definitive references are clause 2.10 and annexes G and S of EN 60950:2000 [41], which describe the minimum creepage distances and clearances permitted between traces for safety reasons.

Clause 2.10 of EN 60950 does not make it very clear that the surge voltages it assumes for mains supplies are based on equipment being installed in an area for which ’Overvoltage Category II’ applies. Annex G gives the levels of surge voltages that are assumed for the various Overvoltage Categories, allowing us to relate transient and surge overvoltages to the minimum creepage distances and clearances specified by clause 2.10 of EN 60950:2000.

If you are not sure what levels of transient or surge voltages might occur on a mains supply, note that EN 60950’s assumption of Overvoltage Category II might be appropriate for most information technology equipment, but it is not necessarily true for equipment in general. Overvoltage Categories I, III or IV may be more relevant, and III and IV are associated with much higher levels of surge overvoltages (up to 8kV), for a given nominal mains supply voltage.

Note that compliance with the surge test requirements in EMC Directive immunity standards does not necessarily mean that equipment will actually withstand the surges it is exposed to in real-life use. 6kV surge voltages can be expected on all single-phase mains outlets between 3 and 300 times a year in the UK (depending on geographical location and on whether the mains supply is provided by

underground or overhead cables) - and other countries are generally as bad or worse - so if you want to make reliable products and reduce warranty costs it will generally be necessary to test mains inputs with surges of at least 6kV, using the IEC 61000-4-5 or (better still) the IEC 61000-4-12 test methods.

6kV is approximately the voltage at which single-phase mains sockets throughout the world generally spark-over, acting as spark-gap protectors for the equipment they power. Mains distribution systems that are only fitted with three-phase sockets will probably have a 'spark-gap' effect at a higher voltage, due to the increased spacing of their terminals, so equipment connected to such networks might need to withstand 10kV surges or more. For more on the real-life surge environment, see [42].

### 7.2 The EMC and safety problems caused by compliance with the RoHS directive

All the guidance on the voltage withstand ability of the gaps between traces, and between a trace and any other metal, is based on the use of '60/40 eutectic' tin/lead solder. But the RoHS Directive [43] bans the use of such solders in all equipment sold in the European Union from mid-2006. Many other countries are also planning to ban the use of lead in solder.

Most companies are treating this simply as a supply-chain issue - just making sure that all their components and PCB soldering processes are 'lead free' - but the problem is that lead-free solders are based on tin, and they grow 'whiskers' over time. Lead was originally added to tin-based solder many decades ago to prevent the growth of 'tin whiskers', but now that it is being removed components and conductors will grow these conductive whiskers. Tin whiskers can short out conductors such as PCB traces, and can reduce the air gap between traces so that they will no longer withstand their rated voltages or transient or surge overvoltages.

A number of manufacturers have applied to the RoHS committee for exemption on the grounds of poor reliability caused by tin whisker growth, but as far as I know no-one has ever commented on the effect of tin whiskers on creepage distances and clearances required for compliance with safety standards such as EN/IEC 60950, EN/IEC 61010-1 or EN/IEC 60335-1 (see [41]) - or on their effect on the ability of a PCB to withstand transient and surge overvoltages for EMC purposes.

Tin whiskers can easily grow to 0.1mm long, and in certain conditions where mechanical stresses are involved, they can grow to 1mm. Since they grow from both conductors across a creepage distance or clearance their net degradation of the voltage withstand of the air gap between conductors is doubled.

The iNEMI report [44] and various other documents show that using a solder based on an alloy of tin, silver and copper (SnAgCu) can - when using controlled manufacturing processes - restrict tin whisker growth to 0.01mm. Unfortunately, it is not known why SnAgCu alloy works so well, which is worrying because it has not yet been proven in all the various physical and climatic environments that equipment (and their PCBs) may be subjected to.

Tin whiskers have the potential to cost manufacturers a very great deal of money, so this article recommends that manufacturers ensure that -
i) all of the 'lead-free' components and 'lead-free' soldering processes they employ only use the SnAgCu alloy and processes recommended by [44]
ii) the minimum spacings between PCB traces (and any other conductors) recommended by [30] or required for safety compliance by the relevant safety standards (e.g. [41]) are increased by *at least* 0.02mm - preferably 0.05mm or more. If not following item i) - increase them by at least 2mm.

Note that the above applies not just for EMC, but also for safety compliance. (Complying with the minimum creepage and clearance requirements of the relevant safety standards will **not** protect your

company from prosecution under safety directives or product liability if tin whiskers cause a safety incident.)

Where explosive atmospheres may be present, the increased possibility of sparking caused by tin whiskers compromising the air gaps between conductors is also a concern.

## 8 EMC-competent QA, change control, cost-reduction

See section 8 of Part 3 of this series [19] for a discussion of this important issue.

Note that PCB layouts should always be reviewed by the electronic designer, who should take all the responsibility for ensuring the layout is good for EMC. The only exception to this rule is when the person doing the PCB layout is competent in understanding EMC in PCBs and applying that knowledge effectively. As discussed in [10] - good modern PCB design for SI and EMC requires a great deal of knowledge and technical expertise and the ability to understand and use computer applications such as field solvers. The level of expertise required can be equal to, or greater than, what is required to design electronic circuits or write software.

## 9 Compromises

It is easy to write an article like this and simply list all of the relevant good EMC design techniques - but in real-life there are a great many design compromises to be made, and this is where the circuit and PCB designers really earn their keep.

Designers are often put under cost or time pressure by managers who don't understand the technical trade-offs, and so don't understand that their actions could have the opposite effect to that which they intend and actually increase project costs and delays, as well as maybe increasing manufacturing and warranty costs. For more on this topic, please refer to part 1 of this series [6], plus the final section of part 2 [8].

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