Another EMC resource
from EMC Standards

6a - Essential PCB design techniques for cost-effective SI, PI, EMC in 2021

Updated for 2021 - Version 6A

Helping you solve your EMC problems

1 Brassey Road, Old Potts Way, Shrewsbury, SY3 7FA T:+44 (0) 1785 660 247 E:info@emcstandards.co.uk

Module 6A
Essential PCB design/layout techniques for cost-effective SI, PI and EMC in 2021

CHERRY CLOUGH CONSULTANTS LTD

emc STANDARDS

Keith Armstrong CEng, FIEE/IET, Senior MIEEE, ACGI, EurIng (Gp1)
phone/fax: +44 (0)1785 660 247
keith.armstrong@cherryclough.com, www.cherryclough.com, www.emcstandards.co.uk

More training courses and textbooks on-line: https://www.emcstandards.co.uk/online-training
Keith's Blog: https://www.emcstandards.co.uk/blog
Linked In: https://www.linkedin.com/in/keith-armstrong-449801172/

Modification Record, v8.1 to v9.0, April 2021

- **The change from v8.1 to v9.0 was needed to improve the terminology and understanding regarding Reference Planes and RF References (RF_{REF}s) but no design guidance has been changed as a result**
- **All slide numbers in all sections re-numbered to remove any letters**
- **Slide 6A.3.7 – rewritten completely to improve terminology**
- ***New slide 6A.3.4 added* (new design guidance on using the newly-defined RF_{REF}s)**
- ***New slide 6A.5.13 added***
- **Slide 6A.6.1 – title changed to use the improved terminology**
- **Slide 6A.6.2 moved to section 3 as slide 6A.3.3**
- **Slides 6A.6.3 through 6.6.7 – rewritten completely to use the improved terminology**
- **Many of the other slides have been changed a little to use the improved terminology, too numerous to list here (but no design guidance has been changed)**

CHERRY CLOUGH CONSULTANTS LTD

emc STANDARDS

Change Record: v7.7 – v8.1, March 2021

- Safety note added to all slides, some re-formatting done as a result
- Very many slides have been improved to help make clear how best to use EM Zoning and the corresponding RF References (RF_{REF}s) *(Note: changed again at v9.0 in April 2021, sorry!)*
- Slide 6A.1.2 – title improved
- Slide 6A.1.7 – helpful new text box added
- Slide 6A.2.2 – URL for purchasing textbook updated
- Slides 6A.3.1, 3.3, 3.4, 3.6 to 3.9, and 3.12 to 3.14 – texts & graphics improved
- Slides 6A.4.4, 4.6 - 4.8, 4.11, 4.13 - 21, 4.24 - 26, and 4.28 – texts & graphics improved
- *New slide 6A.4.29 added* – example of EM Zoning in the X-Box Model X
- Most slides in section 5 have their texts and graphics improved, and have been renumbered from slide 6A.5.50A on
- *Two new slides 6A.5.22a and 6A.5.22b added* – a plane split 'stitching' procedure
- *Eight new slides 6A.6.2 to 9 added* – on controlling resonances when a PCB's structure is different from its RF_{REF} structure
- Version 7.7's slides in section 6: all texts and/or graphics improved, *and* renumbered
- *Five new slides 6A.6.23 to 28 added* – on controlling resonant PCB structures
- Slides 6A.7.2, 7.5-7.8, 7.11, 7.12, 7.16, 7.17, 7.23, 7.25 to 35 – texts & graphics improved
- Slides 6A.8.1, 8.3, 8.10, and 8.27 to 30 – texts and/or graphics improved
- *Two new slides 6A.8.7a and 6A.8.7b added* – on how to parallel large capacitors to reduce their overall self-inductance
- Old slides 6A.9.17-22 moved to 6A.9.30-35; other slides renumbered
- Slides 6A.9.10, 9.11, 9.37 and 9.39 – texts and/or graphics improved
- Slide 6A.10.2, and 10.5 to 10.15 – texts and/or graphics improved
- Slide 6A.11.7 – text improved
- Old 6A.12.5-9 replaced with 6A.12.5-11 *(adding two slides and many new references)*

Good Electromagnetic (EM) Engineering…

– allows cost-effective SI, PI, EMC in design & manufacture

- Our course's guidelines are **well-proven in real-life** to save time & money overall in design and development, and help increase profits & reduce financial risks, for everything, of any size, in all applications…
  see 1.15 and 1.16 in Module 1
  – and can be used in initial design checklists to **DE-RISK a project's SI, PI and EMC** (any relevant guidelines that are not fully applied identify a project risk!) *see 1.16 in Module 1*
- Guidelines based on λ and/or f_{MAX} are for compliance with IEC 61000-6-1 and -3…
  – to adapt them to different EMC standards, see section 1.18 in Module 1: 'The Physics of EMC' *also in Webinar 1d*

Contents

For safety requirements – see our courses on designing for safety compliance

1
Saving time and money

The most cost-effective place to 'fix' EMC, (and SI and PI) – is *in the PCB* !!! (1)

- **The traditional approach of designing/developing a PCB assembly so that it works…**
  - **then trying to pass EMC tests with the whole product by messing around with cabling, shielding and filtering…**
    - **without harming the functional performance or changing the basic shape/size…**
  - **is *guaranteed* to add *unknown* costs and delays…**
  - **and is increasingly likely to require complete redesign (usually only after a great deal of wasted time and money)…**
  - ***if* the market for the product still exists by then!**

The most cost-effective place to 'fix' EMC, (and SI and PI) – is *in the PCB* !!! (2)

- **Applying all these PCB techniques gives good signal integrity (SI), power integrity (PI) and EMC...**
  - **and is much more cost-effective than 'fixing' EMC problems at a higher level of assembly**
- **So although these PCBs often have a higher BOM cost, and need more skill and time to design...**
  - **number of design iterations should be reduced**
    - **time to market should be reduced**
    - **overall-unit-manufacturing-costs should be reduced**
    - **company financial performance should improve**
    - **company financial risks should reduce**

CHERRY CLOUGH CONSULTANTS LTD

emc STANDARDS

Since 2000, time-to-market is now more important for success than BOM cost

- We can't have the ***lowest possible*** BOM cost, *and* the ***fastest*** time-to-market, *and* EMC compliance (i.e. legal sales and low warranty costs)…
  - *without computer simulation tools* *(see my webinar, listed at the end)*
- Less simulation requires longer development...
  - to find out how to achieve EMC compliance with the lowest possible BOM cost…
    - even so, following these guidelines is well-proven to save time and cost overall (compared with not following them)

The required simulation tools include…

- Circuit simulators (e.g. SPICE)
- Signal Integrity (SI) simulators
- Power Integrity (PI) simulators
- EMC simulators
  - not yet able to predict what performance will be achieved on EMC tests, but valuable for optimising design details

- Setting 5 or 10 times tighter design limits into SI and PI simulators helps achieve good EMC
  - but no guarantees!

emc13a v9.0 **All relevant safety requirements must be applied**, not necessarily covered in these slides CCC

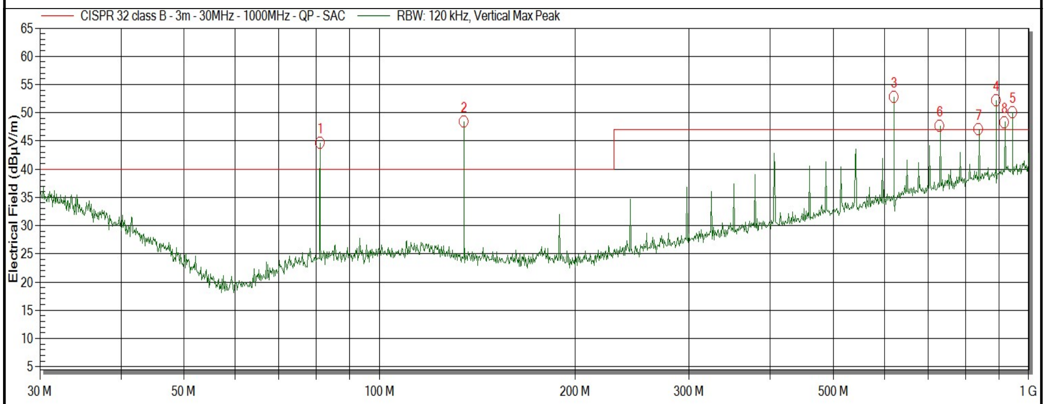
For more detail on saving time and cost, and reducing financial risks, by applying our well-proven future-proof design guidance on SI, PI and EMC…

- see Sections 1.15 and 1.16 in our Module 1 "The Physics of SI, PI and EMC"…
- available as PDF coursenotes and as Webinar 1d both free from emcstandards.co.uk (if you register for free as a Member)

6A.1.6 Cherry Clough Consultants confidential training material 11 of 316

emc13a v9.0 **All relevant safety requirements must be applied**, not necessarily covered in these slides CCC

Emissions from an LVDS driver board after autorouting (with no shielding applied)

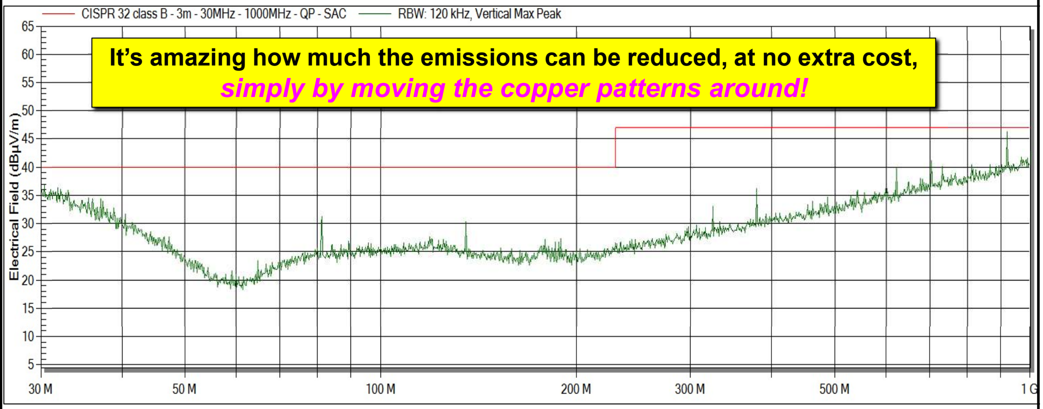


From the results of a laboratory exercise for students organised by Andy Degraeve, Research Assistant KU Leuven, Campus Bruges, M-Group (Mechatronics), Bruges, Belgium, andy.degraeve@kuleuven.be, reported in "*Teaching EMC using an EMC demonstration unit*", presented by Mr Degraeve at APEMC/IEEE 2018, in Singapore

6A.1.7 Cherry Clough Consultants confidential training material 12 of 316

Emissions from same LVDS driver board after manual routing (with no shielding applied)

following: "*EMC for Printed Circuit Boards : Basic and Advanced design & layout techniques*", by Keith Armstrong, Nutwood UK December 2010, ISBN: 978-0-9555118-5-1, only available new from https://www.emcstandards.co.uk/books4 (printed on demand)



From the results of a laboratory exercise for students organised by Andy Degraeve, Research Assistant KU Leuven, Campus Bruges, M-Group (Mechatronics), Bruges, Belgium, andy.degraeve@kuleuven.be, reported in "*Teaching EMC using an EMC demonstration unit*", presented by Mr Degraeve at APEMC/IEEE 2018, in Singapore

2
The scope and application of these design techniques

The textbook that this course is based upon

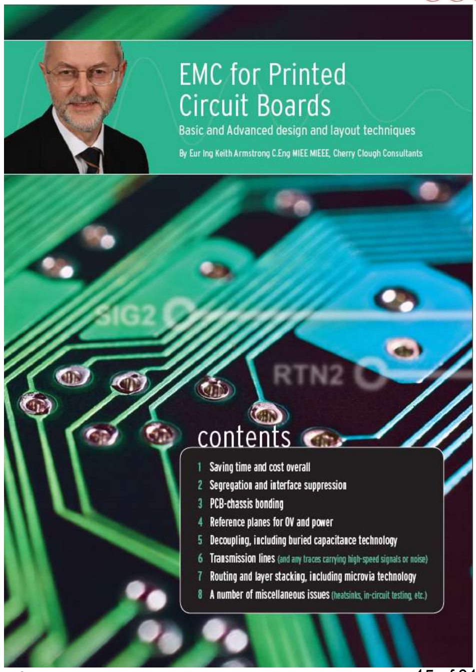
Info and contents list:
www.cherryclough.com

Printed-to-Order from:
https://www.emcstandards.co.uk/emc-for-printed-circuit-boards

***Not* available new from Amazon or any other resellers (who might incorrectly state that it is out of print)**

This book was published in 2005 so is not as up-to-date as this course…

but it does provide a lot more detail on the many techniques that haven't significantly changed since then



This is a basic module

- **This module describes basic Signal Integrity (SI), Power Integrity (PI) and EMC techniques for PCB design / layout…**
  - **and, because *all* conductors behave as accidental transmitting/receiving antennas, many of these could be described as 'anti-antenna' design techniques…**
  - **– now essential for all PCBs, whether they carry analogue; digital; switch-mode, or mixed technologies**
- **The Advanced PCB SI, PI & EMC Techniques course (Module 10A, www.emcstandards.co.uk/advanced-pcb-design-for-cost-effective-si-pi-an) is needed for high-speed data processing because even very small conductors (electrical, mechanical, etc.) become very efficient accidental antennas**

This module deals mostly with 'what'

- **Issues such as 'why' are not covered in depth…**
  (see Module 1, or my book: "the Physical Basis of EMC", referenced at the end)
  - **but all the techniques described here are widely used by successful manufacturers…**
  - **and very well proven in practice worldwide, in all applications, many of them for over 30 years…**
    - **and SI, PI and EMC academics and other experts explain why they work so well**
- **There are a great many non-PCB design techniques for cost-effective SI, PI and EMC, covered in our other training course modules, articles and books**

Use the following slides as a checklist

- **Just like a road trip: deviating from the optimum route will generally cause problems…**
    - **in this case: delayed time-to-market; increased overall unit manufacturing cost; increased warranty costs…**
  - **so use these guidelines to identify which design areas need attention because they can't be fully applied…**
    - **this helps avoid the "unknown unknown" problems that can damage or even ruin a project at a late stage**
- **If any of these techniques can't be fully applied, do something else to deal with the SI, PI, EMC issues…**
  - **or warn your managers about the inevitable increase in the financial and timescale risks**

If you don't see your favourite design or layout technique in these slides...

- then it probably isn't good any more, for SI, PI or EMC !!
  - especially splitting planes and 'single-point earthing or grounding' (sometimes called 'star earthing/grounding'), and the use of galvanic isolation where not needed for safety
  - I recommend reading these notes through carefully to see what they do and don't recommend – to 'flush out' any old-fashioned assumptions

- ***All*** applications increasingly suffer more RF noise from the worsening external environment…
  - and die-shrinking (Moore's Law) is continually making ICs both noisier *and* more sensitive, to ever-higher frequencies…
    - so design for SI, PI and EMC has to keep evolving to keep pace — *whether we want to, or not!*

Wavelength λ is very important in PCB design

- Frequency (f), λ, and velocity of propagation (v) are related by: $v = f \cdot \lambda$
- In vacuum or air: $v = c = 3.10^8$ metres/second so $\lambda = 300/f$ (f in MHz gives λ in metres; f in GHz – λ in mm)
- But v is slower in PCB traces, because $v = c/\sqrt{\varepsilon_r}$ where ε_r is the dielectric constant, so $\lambda_{PCB} = 300/f \cdot \sqrt{\varepsilon_r}$
  - and in FR4, $\varepsilon_r \approx 4$ (above 1MHz) making v and λ approximately half what they are in air, so for FR4 PCBs we generally assume: $\lambda = 150/f$
  - FR408 for lead-free soldered boards (higher soldering temperature) has a dielectric constant approx. 90% of traditional FR4, which is only slightly significant for design of matched transmission lines