Another EMC resource
from EMC Standards

10a - Advanced PCB design techniques for cost-effective SI, PI and EMC in 2022

Updated for 2022

Helping you solve your EMC problems

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Module 10A
Advanced PCB design/layout techniques for cost-effective SI, PI and EMC in 2022

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Good Electromagnetic (EM) Engineering…

– **allows cost-effective SI, PI, EMC in design & manufacture**

- **Our course's guidelines are well-proven in real-life to save time & money overall in design and development, *and* help increase profits & reduce financial risks, for everything, of any size, in all applications…**
  see 1.15 and 1.16 in Module 1
  – **and can be used in initial design checklists to DE-RISK a project's SI, PI and EMC (any relevant guidelines not fully applied are a project risk!)**
  see 1.16 in Module 1
- **Guidelines based on λ and/or f_{MAX} are for compliance with IEC 61000-6-1 and -3…**
  – **to adapt them to different EMC standards, see section 1.18 in Module 1: 'The Physics of EMC'** *also in Webinar 1d*

Contents

This Module 10A is a continuation of Module 6A, and should not be used without it

For safety design, see: www.emcstandards.co.uk/the-safe-design-of-electrical-equipment-lvd-com

Contents continued...

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The textbook that this course is based upon

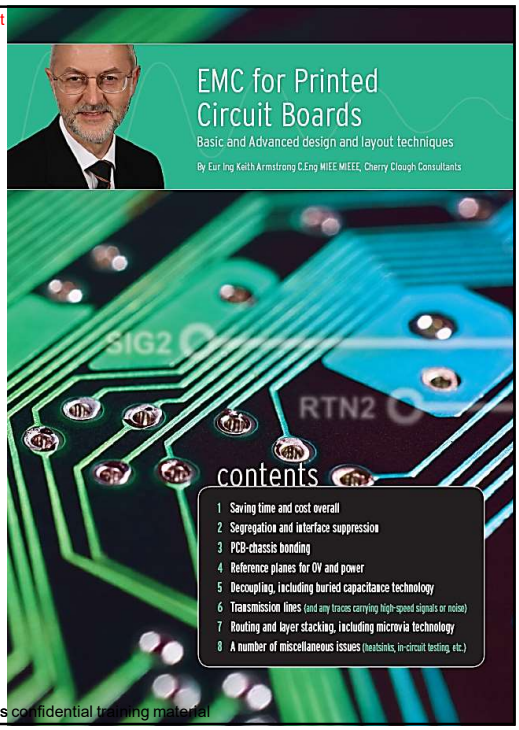
Info and contents list: www.cherryclough.com

Printed-to-Order from:
www.emcstandards.co.uk/books4

***Not* available new from Amazon or any other resellers (who might incorrectly state that it is out of print)**

This book was published in 2005 so is not as up-to-date as this course…

but it does provide a lot more detail on the many techniques that haven't significantly changed

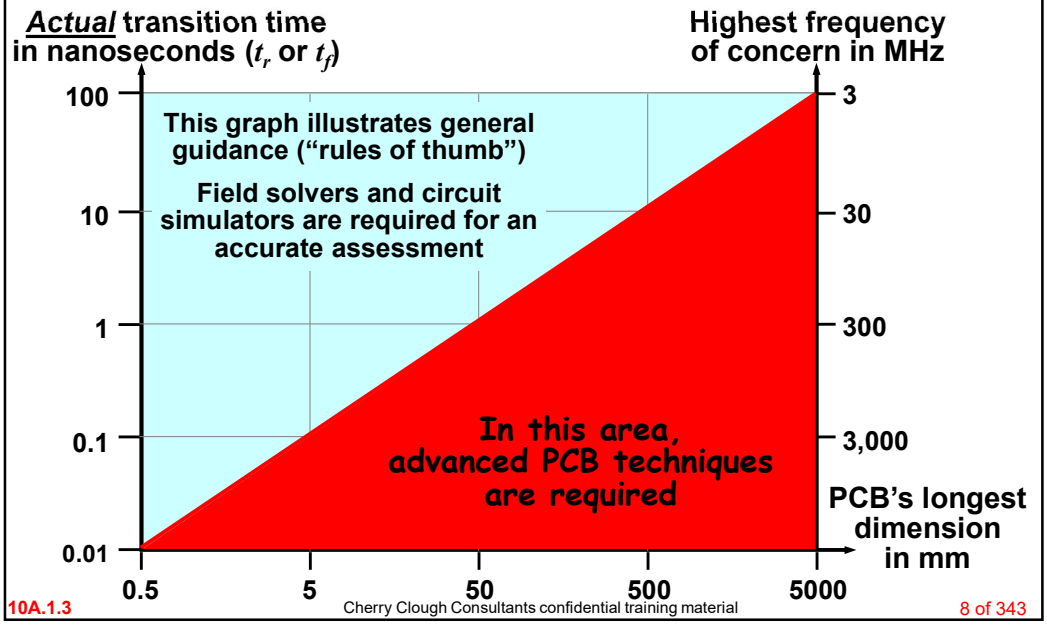


1
When should we use advanced PCB techniques?

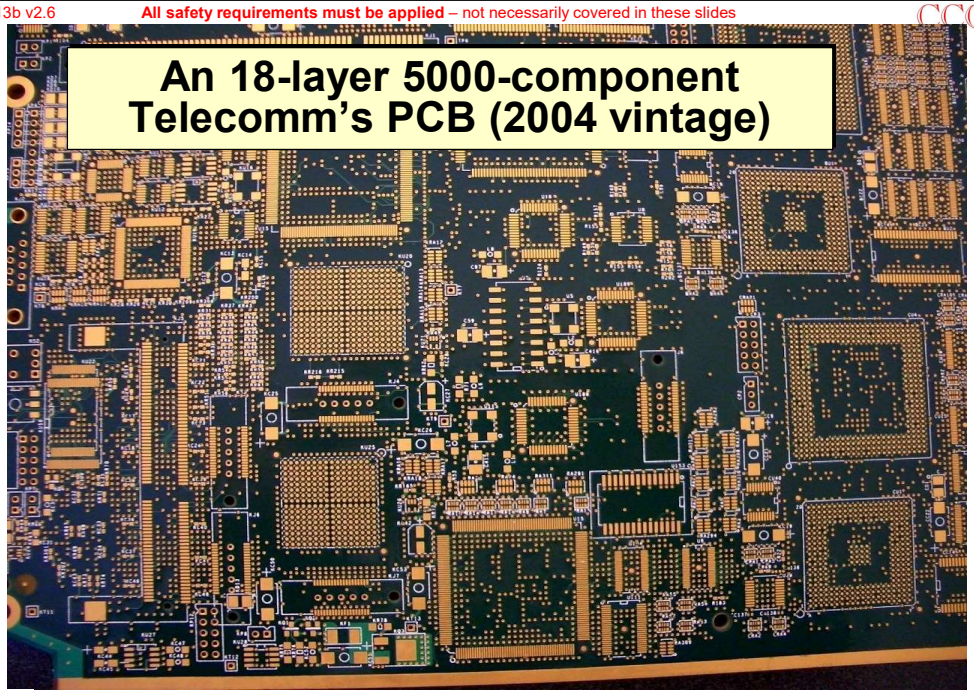
Advanced PCB techniques help to…

- Reduce cost by eliminating enclosure shielding (or at least reducing its specification and cost)…
- Reduce interference with co-located wireless datacoms (e.g. increase receiver range for GSM, GPRS, 3G, 4G, 5G, Bluetooth, Zigbee, LoRa, etc., etc.)…
- Allow co-located GPS to see many more satellites…
- Use RF power devices (including isolating DC/DC)…
- Make high-speed processors / DSP function correctly (achieve good signal integrity, SI, and power integrity, PI)…
- Use the latest IC technologies (e.g. 5nm or smaller silicon processes), BGAs and 'chip scale' packages…
- Reduce time to market and compliance costs

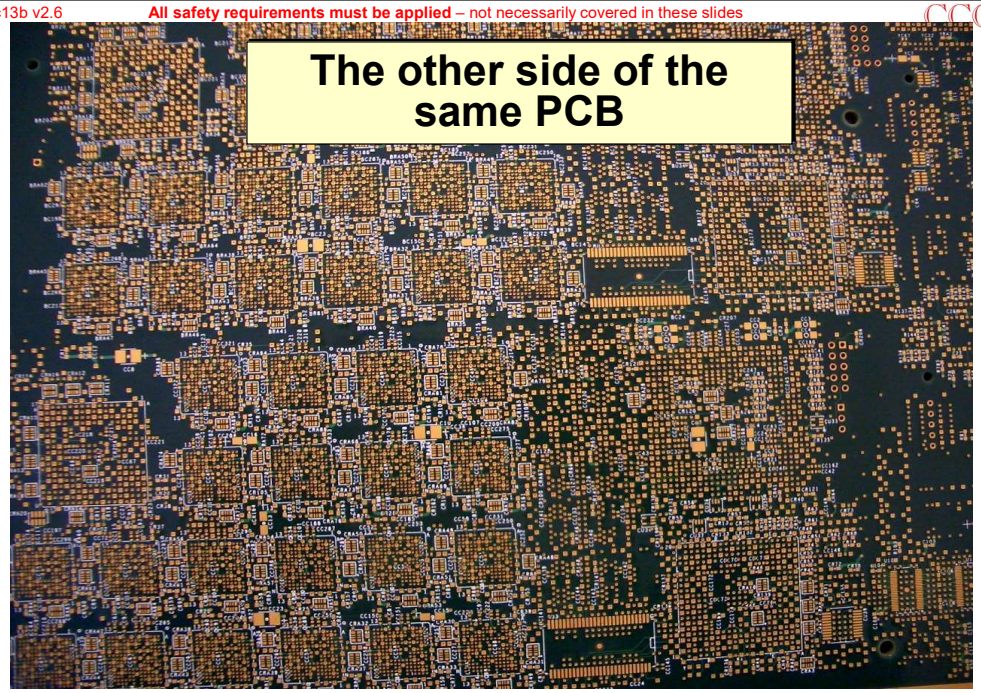
When do we need advanced techniques?



An 18-layer 5000-component Telecomm's PCB (2004 vintage)

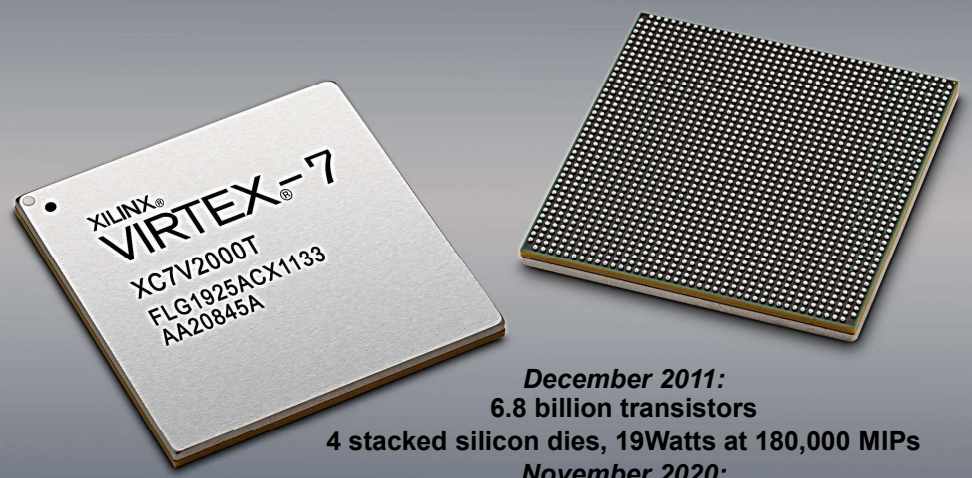


The other side of the same PCB



2
Future trends and their implications

Future trends



December 2011:
6.8 billion transistors
4 stacked silicon dies, 19Watts at 180,000 MIPs
November 2020:
Apple's new 5nm A14 processor has a transistor density of 134 million transistors/mm^2

IC trends

- **IC trends are driven by:**
  - **increasing processing power...**
  - **increasing complexity (more transistors per square mm)…**
  - **improving wafer yield…**
  - **reducing cost**
- **All these are achieved by shrinking the feature sizes on the silicon wafers…**
  - **now (2022) at 5nm, with even smaller processes still being developed *(see next)*…**
  - **an unstoppable trend towards smaller feature sizes**

The ITRS 2007 roadmap

www.itrs2.net

(copied from "Power Integrity and EMC Design for High-speed Circuits Packages", by Prof. Tzong-Lin Wu, Ph.D., National Taiwan University, EMC DL 2009 (IEEE EMC Distinguished Lecture, Netherland/Belgium/Luxembourg Chapter, June 18, 2009)

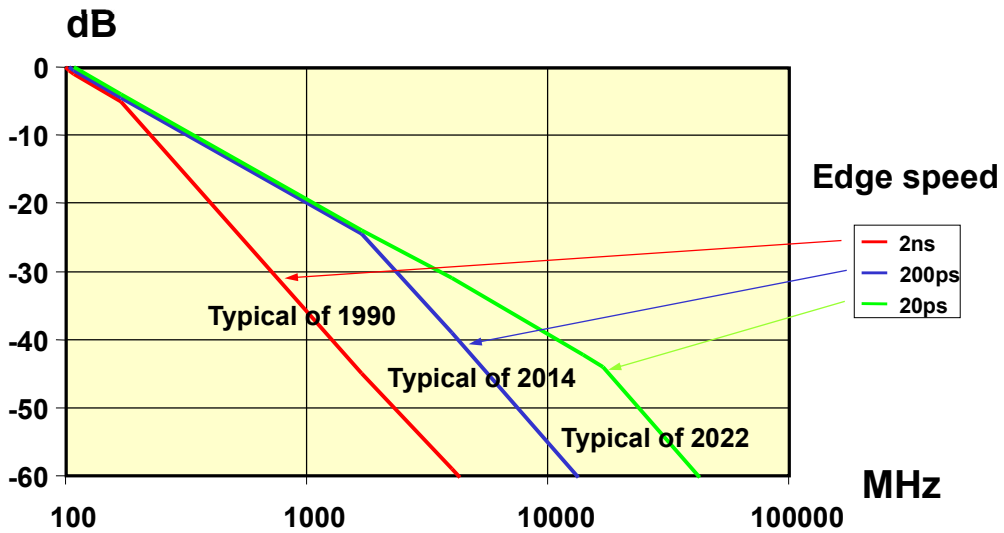
Year	Feature	V_{dd}	Chip Freq.	Power
2007	68nm	1.1V	4.70GHz	189W
2010	45nm	1.0V	5.88GHz	198W
2013	32nm	0.9V	7.34GHz	198W
2016	22nm	0.8V	9.18GHz	198W
2019	16nm	0.7V	11.48GHz	198W
And from the ITRS 2013 Roadmap:				
2021	12nm	0.74V	7.53GHz	–

TSMC looks to 2nm in 2024 Business news: April 18, 2022 www.eenewseurope.com/en/tsmc-looks-to-2nm-in-2024
With 3nm volume production starting later this year, TSMC is turning its attention to the 2nm generation. Both are being driven by demand for chips for high performance computing, says CC Wei, CEO of TSMC in its latest quarterly results, Advanced technologies below 7nm account for half the company's revenue…

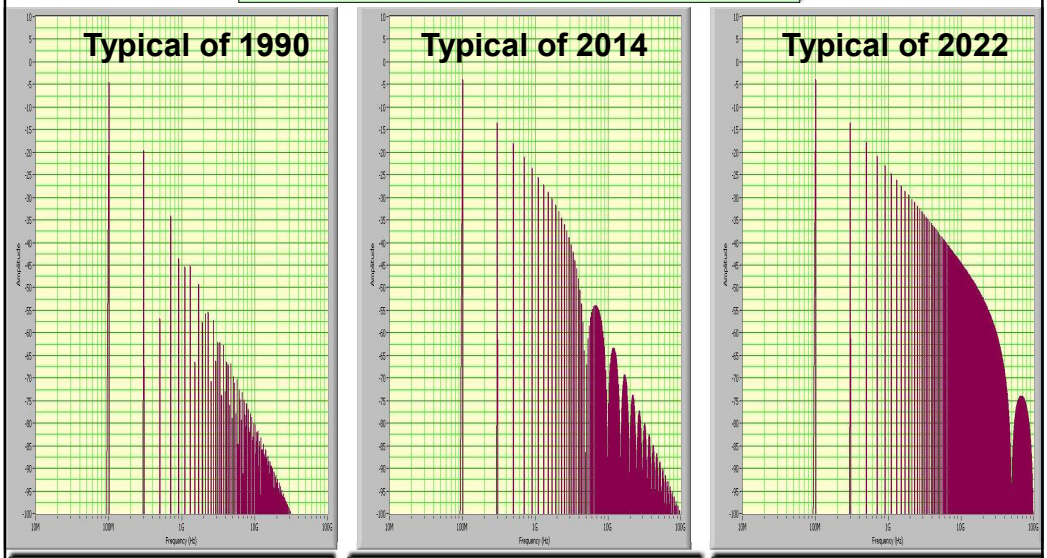
EMC effects of shrinking the feature size of transistors in ICs

- ICs become more susceptible to over-voltage damage…
  - because their insulation is thinner/narrower
- Data 'bits' are more vulnerable to data corruption…
  - due to the wider bandwidth and lower capacitance
- Increasing emissions
  - smaller feature sizes means less capacitance
    - means faster switching edges
    - means more energy in richer harmonic spectra
    - *even if the clock frequency doesn't increase*

Effects of switching edge speed on the harmonics of a 100MHz clock



Simulating clock spectra, 10MHz – 100GHz (courtesy of Allan Diamond)



100MHz clock, 2ns edge | 100MHz clock, 200ps edge | 100MHzclock, 20ps edge

Shrinking feature size affects *all* ICs

- **All ICs (not just new ones) migrate to the new silicon fabrication processes with smaller feature sizes…**
  - **to improve the yield from each silicon wafer, to make more money for the semiconductor manufacturer**
- **Buying the same old devices in the same old packages doesn't protect from these 'mask-shrunk' ('die shrunk') devices…**
  - **a new batch of ICs can make a product non-compliant for EMC emissions and/or immunity…**
    - **which has cost several companies millions of dollars, and made one (that I know of) with 1,000 employees be recommended for bankruptcy**

IC packaging trends

- The trend to smaller IC packages can also create EMC problems…
  - smaller packages have lower inductances in their bond wires and lead frames….
  - allowing faster digital signal edges, and more 'core-logic noise', to appear at the IC's PCB connections
- Smaller IC packages *can* help *improve* EMC…
  - ***but only*** when appropriate advanced PCB EMC techniques and technologies (e.g. HDI, microvia) are fully applied in the design

The trend to lower supply voltages

- For higher speeds (and lower power dissipation) ICs and datacoms are using increasingly lower power rail voltages…
  - which require lower logic threshold voltages
- So a PCB that used to work, can fail when lower-voltage ICs are fitted, *even though the circuit and clock speed is unchanged…*
  - simply because the existing noise levels now exceed the new (lower) logic thresholds…
    - but the new ICs probably have higher noise levels too

see "The Project from Hell" on the next slide….