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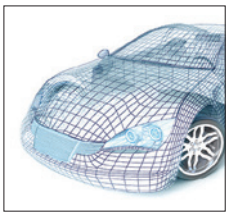
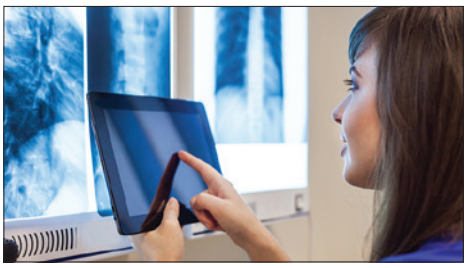
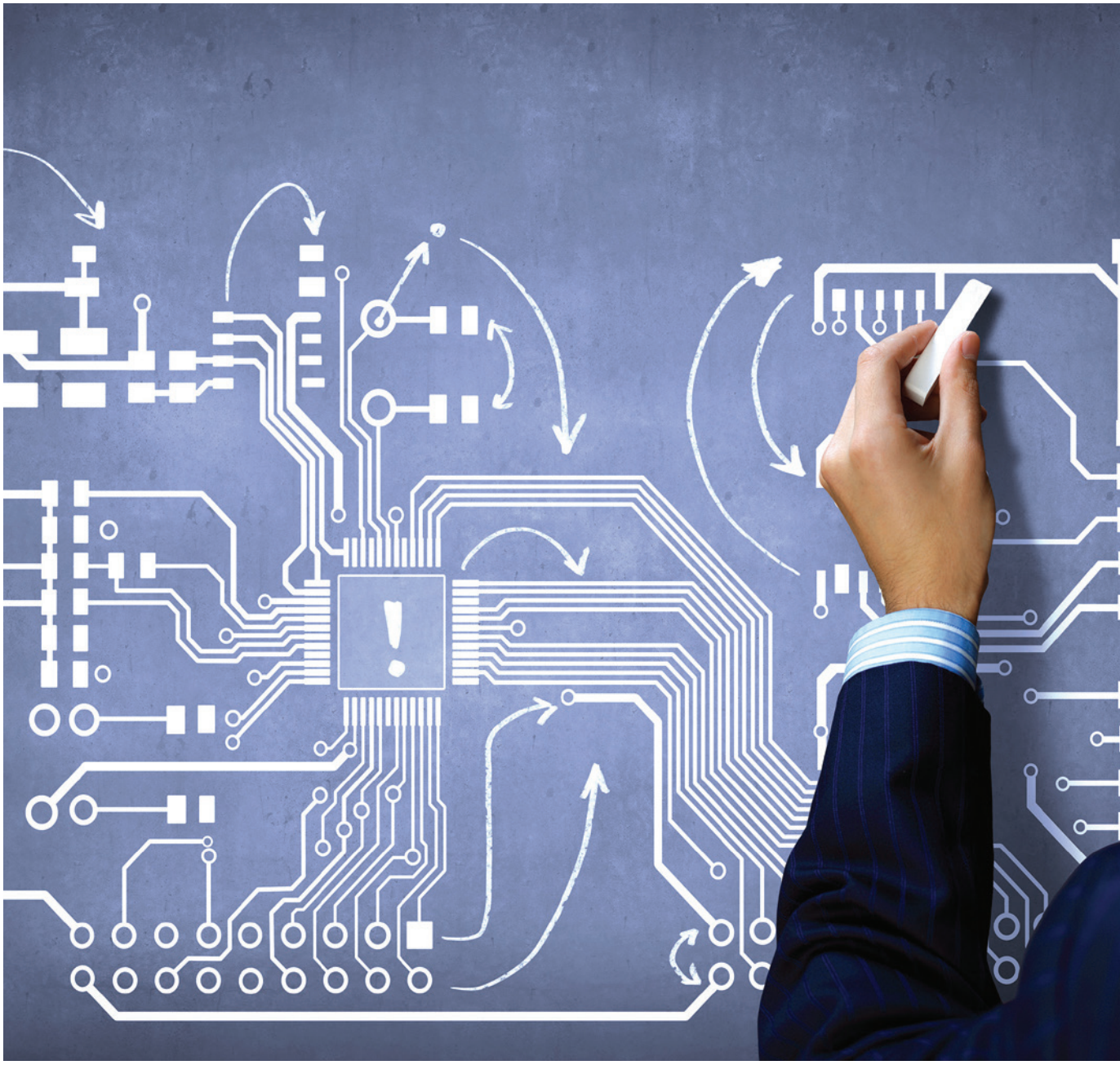




INTRODUCTION TO "EM ENGINEERING"



Keith Armstrong is the founder and principal of Cherry Clough Consultants Ltd, a UK-based company that utilizes field-tested EMC engineering principles and practices to help companies achieve compliance for their products and reduce their potential risk. He is a Fellow of the IET and a Senior Member of the IEEE, and holds an Honours Degree in Electrical Engineering from the Imperial College, London (UK). Keith can be reached at keith.armstrong@cherryclough.com.

By Keith Armstrong

Achieving electromagnetic compatibility (EMC) compliance is now straightforward, quick, and easy – using the EM Engineering process that I will describe in this article.

We all know that radio communication is propagating electromagnetic (EM) waves, but not many electronic designers realize that all electricity is actually propagating EM waves too. This means all electronic signals, controls and data, even 50/60Hz power.

Achieving signal integrity (SI) and power integrity (PI) compliance is even easier than achieving EMC, because their design requirements are not as tough as good EMC design. So using good EMC design techniques from the start of a project automatically takes care of SI and PI.

When we learn circuit design, we learn the *children's* version of electricity. This is the version in which charge carriers shuffle along conductors, creating currents that flow from the positive power rail to the "ground" or 0V, or to the negative power rail. The Spice simulators we have on our desktops appear to confirm this design approach, but ignore the fact that all electrical currents are actually propagating electromagnetic waves in real life.

This distinction might not have mattered very much for (non-radio) designers in the 1950s and 1960s, but it started to become important in the 1970s when microprocessors began to be used. The very rapid development in electronics and electronic devices since then, means that every circuit, even audio-frequency analog, is now unavoidably polluted with radio frequency (RF) noises from the harmonics of digital and power switching waveforms, and wireless data communications.

The radio frequencies we cannot avoid using are now so very high, and their wavelengths so small, that the children's version of circuit design can only be the starting point for a real product's circuit design – one that fully achieves all of its functional specifications (i.e., complies with its SI and PI requirements) and also complies with its EMC requirements, preferably on its first prototype.

At the time of writing, a set of computer software applications that can be used to *guarantee that a* circuit design on a PCB will meet its functional performance on its first prototype costs in the region of $250,000 (US). When used with some EMC design competence, such simulators can also help ensure EMC compliance.

These simulators were first developed for PC motherboard manufacturers during the 1990s, when motherboard sales lifetimes were just 90 days. At that time, they cost $1 million (US) per seat – but if you wanted to be a real player in the PC motherboard industry you couldn't afford the time to re-spin your PCB designs, so had to pay this price.

Even these days, $250,000 (US) seems like a lot of money, but in fact it is easy to justify financially because of its very short payback period (see [1]). Please don't forget that using these simulators effectively requires sufficient training and regular use.

When using such a simulator, I recommend using a design process I call "EM Engineering" as a "ballpark" check on its results. It is so easy to misplace a decimal point when entering data, resulting in a "garbage in, garbage out" situation which – without what is sometimes called "sanity checking" – might not become obvious until a lot of cost and time has been wasted.

However, the EM Engineering process described in this article can be used without any computer simulators at all. Even start-up, one-man-band companies operating from their garages (just like Hewlett Packard started out) with very little money at all, can use it to get their SI, PI and EMC right on their first prototypes.

WHAT IS EM ENGINEERING (EMGINEERING), AND WHAT ARE ITS FINANCIAL BENEFITS?

EMgineering is a design process that makes it possible to either avoid or deal with the weird and wonderful things that happen when circuit components start to behave other than their "lumped" characteristics (e.g., 1kΩ resistor, 1nF capacitor), because of our unavoidable and ever-increasing use of ever-higher radio frequencies.

Since 1998, I have been publishing and presenting material on how to do good, cost-effective SI, PI and EMC design (see [2] [3] [4] and [5]). It took me over 30 years to learn to do this, and to be able to describe it in a way that a competent electronic engineer can quickly understand and apply successfully. But in recent years I have had the feeling that my descriptions were incomplete.

While I was helping customers to achieve good EMC design, I began to notice that I was automatically using certain techniques that my publications and presentations had not then explicitly described. Only during the last few months have I been able to find the words and graphics to describe these additional techniques (the subject of this article) and in November 2016 I felt able to add them to my training course on "The Physical Basis of EMC." Since then I have created a freely available webinar on "EMgineering," [6], but this article is the first time that this new design information has been published in print media.

It is very important to understand that *EMC is an important financial risk issue.*

It is a common management mistake to treat EMC as only being a regulatory issue (to be just-about complied with, or avoided if possible). In real life, products which don't comply with all of their relevant EMC emissions and immunity standards tend to have poor functional performance and be unreliable. This leads to high levels of warranty costs and poor customer perception. In other words, they are not good products for a company that wants to be financially successful and/or have a good future.

The aim of the EMgineering approach is to save cost and time to get to market more quickly with products that have lower overall costs of manufacture, thereby reducing financial risks and increasing profitability in all electronic applications. Because all of our electronics industries, and industries which use electronics, exist for the sole purpose of making money, EMgineering is very important for their financial success.

Over the last 20 or more years, some manufacturers have used these EMC design guidelines to dramatically reduce their time-to-market, design/development costs, overall unit manufacturing costs, and warranty costs. A very recent example is this large weatherproof outdoor video display, the Barco R Series, launched in 2016. It has a matrix of SMD LEDs on a very large three-layer flexible PCB without a plane layer or any kind of shielding, communicates data using 1000-BaseT Ethernet, and has powerful image processing functions.

The example shown in Figure 1 has LEDs on a 10mm pitch, is 3.9m (nearly 12 feet) tall, and has 2.3kW of mains power to DC conversion – most of which

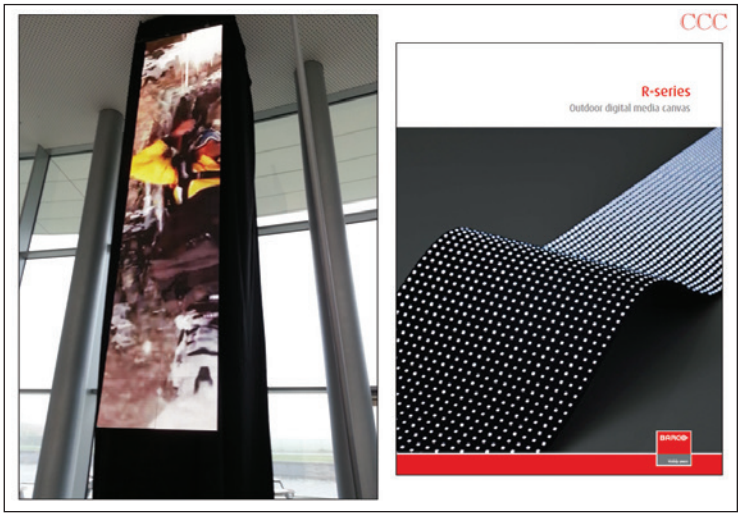


Figure 1: The Barco R10, 3.9 metres tall (more than 12 feet)

goes to drive the LEDs. These types of outdoor displays (see Figure 1) are often stacked horizontally and/or vertically to create larger video displays, for example for football and baseball stadiums. Because the R series has one-quarter the weight and one-tenth the thickness of all previous outdoor displays of comparable size, and is flexible, it is very much easier, quicker and less costly to install or de-install on a building or other structure.

My EMgineering design techniques were rigorously applied right from the start of the R Series project. The result was that – despite there being no shielding used anywhere in this product – its first production prototype easily met its required emissions standard! Its designers were very pleased indeed, and so were their managers.

USING GOOD EMC DESIGN GUIDELINES AS A CHECKLIST

My EMC guidelines are best used initially as a design checklist (see [7]) to identify SI, PI or EMC risks so that a project can be de-risked early on when design changes are very quick and inexpensive, instead of having to make very slow and very costly changes after failing EMC tests towards the end of a project.

Where a design guideline can be fully applied without compromise, it should be. Where a design guideline cannot be fully applied, this identifies an issue which needs careful design to avoid increasing the project's risk. Designers should then do something else that deals with the SI, PI, EMC issues. Where management do not permit the use of a suitable compromise (for example, due the common, but often misguided, idea that lower bill of material costs are needed for higher profits (see [8]), it must be understood that this will inevitably increase the project's financial and timescale risks. I strongly recommend that all such decisions are recorded in the minutes of design reviews that are signed by the manager who made them, so that they can't in the future blame the designers for the increased delays and costs caused by their decisions.

If you don't see your favorite design technique or guideline in my EMgineering design practices, then it probably isn't a good one any more, for SI, PI or EMC. Especially bad is the practice of "single-point earthing/grounding" (sometimes called "star earthing/grounding") – even in low-frequency applications, for example low-frequency instrumentation and audio from DC to 20kHz. This is because, as I said earlier, all electronic applications

are without exception increasingly suffering more RF noise, due to worsening external EM environments and developments in semiconductors. Even undersea electronics must now be designed to cope with the undersea EM environment!

So let's now begin to explain in greater detail the EMgineering design concepts.

CONTROLLING RETURN CURRENTS WITH METAL PLANES

All currents always flow in closed loops, whether they are DM currents (i.e., differential mode: wanted signals and power) or CM currents (i.e., common mode: unwanted, stray, parasitic, sneak, etc.). Always have, always will; no exceptions, ever; at least in this universe.

This is why electronic circuits can work perfectly well with excellent SI, PI and EMC even without being connected to metal rods stuck in the true earth/ground (the soil that we grow plants in, play sports on, and build roads and buildings on).

DM and CM currents naturally flow in the loops with the lowest impedance, which are also the loops with the least stray E, H and EM fields, giving the best SI, PI and EMC for any design of conductors and insulators. This was discovered by Michael Faraday in the 1700s, although of course he had never heard of SI, PI or EMC.

Faraday's Law of Electromagnetic Induction later became one of Maxwell's famous four equations, but I'd be prepared to bet that no one reading this article who was taught Maxwell's Equations at University ever heard their lecturer describe Faraday's Law in such practical, useful engineering terms.

This means that we don't have to struggle to make our currents flow in the paths with the least stray fields – the best SI, PI and EMC – because they do it automatically. If our product is suffering from too much stray "RF noise leakage" (or stray "RF noise pick-up"), it is often because we didn't provide it with paths having low-enough loop impedances for its DM and CM return currents [9].

Nearby metal planes make ideal low-impedance current paths, and below I show how our designs can use this to huge advantage by combining a single unbroken reference/return plane for all circuits, with "EM zoning."

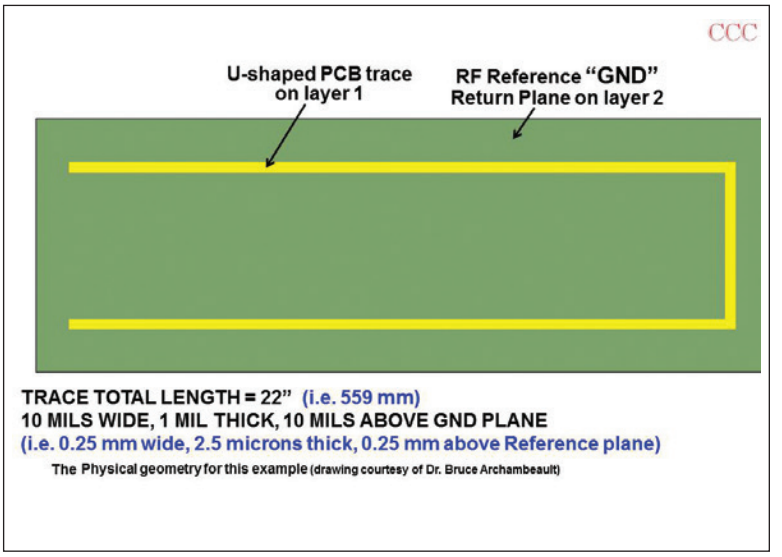


Figure 2: Computer simulation of a U-shaped trace with a solid PCB plane as return path

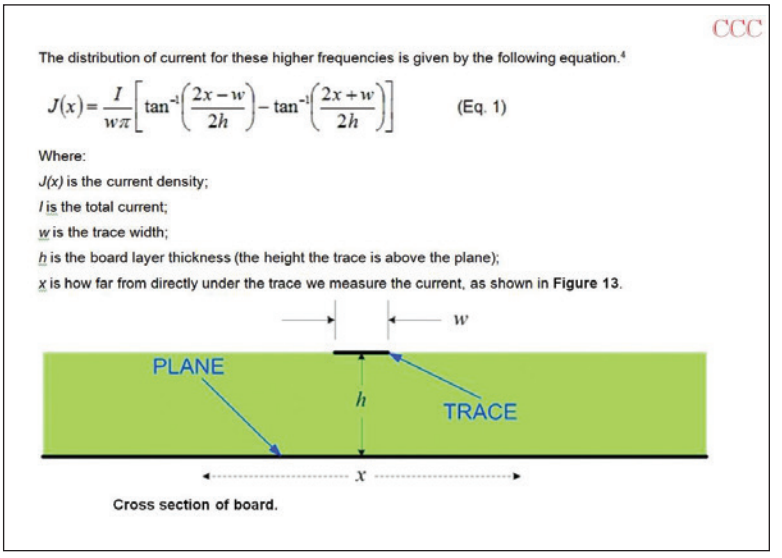


Figure 3: Details of the simulation of Figure 2

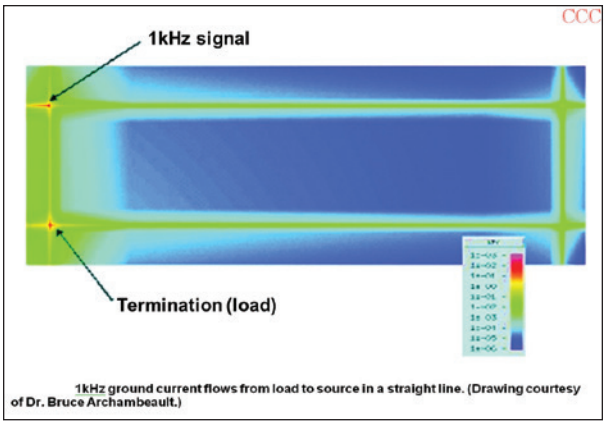


Figure 4: Simulating Figure 2's current densities at 1kHz

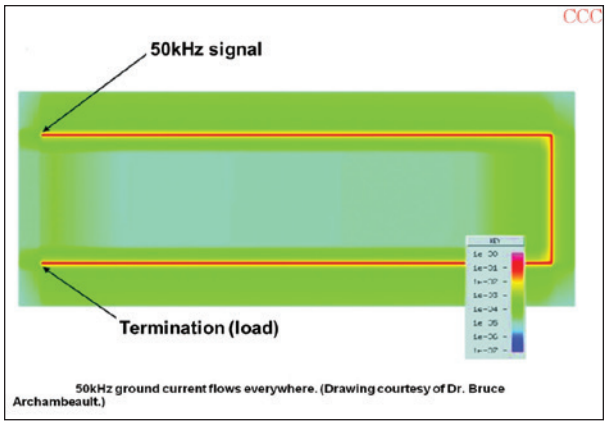


Figure 5: Simulating Figure 2's current densities at 50kHz

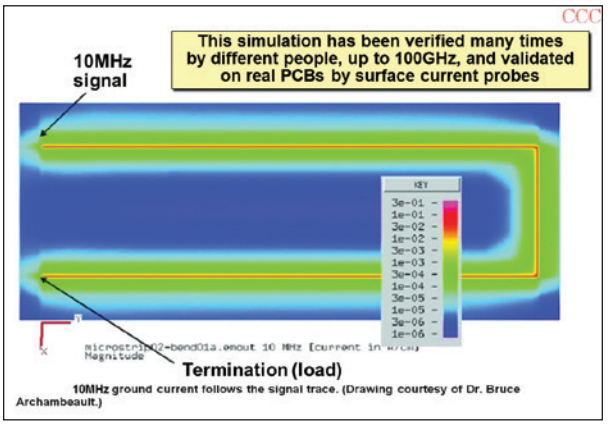


Figure 6: Simulating Figure 2's current densities at 10MHz

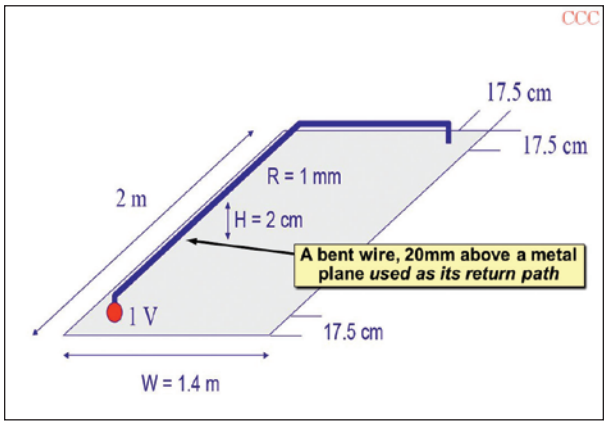


Figure 7: Details for the simulation of Figure 8: a wire using a steel chassis for its return current

Michael Faraday would have been more than thrilled to have seen the computer simulations in Figures 2-8 (from [16] and [17]). Such simulations are commonly seen in the world of EMC academia, but rarely seen in the world of electronic design.

These figures show that segregating circuits into individual areas, which I call EM zones (EMZs), and keeping their components and conductors very close to a single metal return (reference) plane, helps ensure that the return currents for one EMZ do not interfere with the circuits in other EMZs.

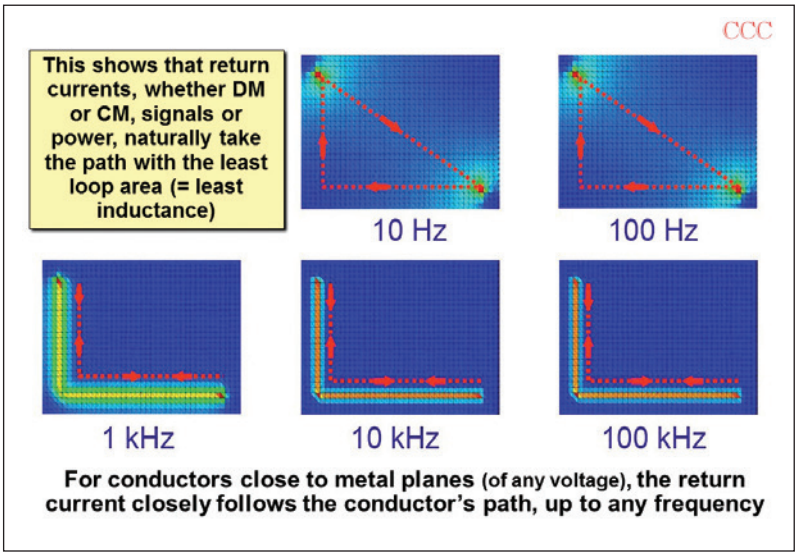


Figure 8: Computer simulations of return current densities for the wire above a steel chassis (the red dotted lines show the average of the current flows, and were drawn by hand

This single reference plane for all circuits is usually at 0V potential – but not always, for example, electricity power consumption metering circuits generally use the live lead of the mains supply as their reference plane.

Designers often call their circuit's reference/return conductor Ground, GND, Earth or Chassis, but because of the potential for confusion with safety grounding/earthing, I don't recommend using these words, or the symbols associated with them, for anything other than actual physical connections to the safety ground, protective earth, or vehicle chassis. The use of such inappropriate words and drawing symbols in electronic circuit design has cost many companies many millions of dollars in delays, design re-spins and lost sales over the decades, and still is.

A single unbroken reference plane, with no splits or gaps in it, underlying all of a circuit's components and conductors (in fact, extending beyond them where possible), and very close to all the components and conductors, provides the best current return path for SI, PI and EMC.

Splits and gaps in reference planes used to be acceptable, and even used to be recommended in many EMC textbooks and training courses written before 2000. However, these days and for the future, any splits in reference planes are likely to resonate at the very high RF frequency DM and CM noises unavoidably emitted by microprocessors, FPGAs, and wireless data communications, causing problems for EMC compliance and possibly for SI and PI too. In some applications (particularly cellphones) it is already the case that the clearance holes around the vias in through-hole-plate (THP) PCB manufacturing technology cause too many problems for SI, PI and EMC. Indeed, I fully expect that THP board-manufacturing technology will not last much longer. Like all previous board-manufacturing technologies, one day it will only be used in very low-technology products.

Using EM zoning and relying on return currents staying within their circuits' individual EMZs, I haven't split a reference plane since 1981 (except for galvanic isolation) on many hundreds of different PCBs for a huge range of different applications, worldwide. They all achieved excellent SI, PI and EMC – even those with very powerful digital processing, very powerful DC/DC, and very sensitive circuits on the same PCB!

These included low-frequency instrumentation and professional audio circuits which – with my EMC design techniques applied – usually achieved better functional specifications despite having microprocessors and DC/DC switching converters on the same PCB than when they had been all-analog and used single-point/star grounding techniques.

Any single-point/star grounding system should now be understood as a bunch of RF resonating antennas, and – if used – designed on that basis.

If you are concerned that Figures 2-8 show that at lower frequencies – where the path of lowest loop impedance is dominated by resistance – the return currents from one circuit zone can flow through the reference plane area of another, please bear in mind that the resistance of a metal plane is very low indeed, very much lower than a wire or PCB trace would be, so the noise voltage dropped across any area of the reference plane is very low indeed at such low frequencies.

If this noise voltage is not low enough, it can be reduced by paralleling PCB planes and/or by multipoint electrical bonding to a thicker metal plate (usually part of a structural chassis, frame, or other enclosure) (see [10]).

However, I hope it is obvious that, if the resistance-dominated (i.e., low frequency) return currents are so very large that even the mitigation techniques discussed in [10] are inadequate for the noise floor of a sensitive circuit sharing the same reference plane, other steps should be taken to mitigate the problem. You might even choose to split the plane to divert the low frequency currents away from the sensitive circuit, always bearing in mind that the split is a resonant slot antenna, and designing around the resulting issues.

(As described in the PCB design guidelines in [2] [3] and [4], it is important to "stitch" across such reference plane splits with capacitors spaced $<< \lambda/10$ at f_{MAX} apart (see later), or use embedded capacitance inside the board, to try to achieve the benefits of a solid plane at radio frequencies whilst the split prevents the flow of low-frequency currents in undesirable areas.)

EM ZONING (SOMETIMES CALLED CIRCUIT SEGREGATION)

EM zoning can be simply summed up like this: we don't allow any frequencies in an EMZ which can't easily cope with them. This is why many good SI, PI or EMC design techniques could be described as "anti-antenna" and/or "anti-resonance" techniques.

Whether conductors are electronic, electrical or mechanical, and not forgetting conductive liquids in pipes, they are all accidental RF antennas. They all couple EM noise energy by conduction and/or by radiating fields: electric (E), magnetic (H or M), and electromagnetic (EM), whether we want them to, or not. It's what all conductors do, if left to themselves! They are especially effective accidental antennas at their resonant frequencies, and at frequencies near to their resonant frequencies, whether their resonance is caused by their circuit/component values (e.g., $1/2\pi\sqrt{(LC)}$ resonances), or by their structural dimensions.

All real components and devices have stray resistances, inductances and capacitances, which severely change their impedance and their circuit's behavior above some frequency (see the "Choice of Components" section in [11]). These include strays which are intrinsic to the component itself (e.g., the ESL of a capacitor or resistor), and strays which are associated with the conductors that interconnect them (series inductance and resistance) and with their insulators, such as fiberglass, PVC, air (stray capacitance, mutual inductance, antenna-mode behavior, etc.).

Unwanted circuit resonances should be avoided by taking the effects of these strays into account during circuit design, for example by using Spice simulation with all identified strays included, using first-order, second-order, etc., models for the components, depending on f_{MAX} (discussed later), propagation times, coupling factors, etc.

Even better would be for the Spice simulator to also take into account the stray Rs, Ls, and Cs; propagation times; stray electric field (E) and magnetic field (M) couplings, etc., associated with the PCB layout, cabling and mechanical structures. These can be estimated, but ideally should be extracted from the 2-D and 3-D drawings of the assembly, using suitable field-solvers (and doing this is an essential part of the $250,000 simulators I mentioned earlier).

In addition to preventing unwanted resonances within the circuits themselves, it is also necessary to prevent unwanted resonances that arise due to the physical dimensions of conductor and dielectric structures. This is another reason for using EM zoning: ensuring the dimensions associated with each EMZ are as small as practical, so that the resonant frequencies associated with their dimensions are as high as possible – hopefully much higher than f_{MAX}. Where we can't avoid unwanted structural resonances, we generally dampen them down to minimize their bad influences on SI, PI or EMC.

We attenuate EM noises with EM mitigation techniques such as shielding, filtering, ESD and transient suppression, galvanic isolation, etc.; the practical cost-effective design of which has been detailed in my other publications and presentations.

Effective use of any EM mitigation depends upon effective EM zoning. Otherwise, the performance of the mitigation measure is degraded by EM noise that propagates and/or couples from one side of the mitigating device or structure, to the other side.

Shields, filters, suppressers, galvanic isolators, etc., cannot work (at least, not very well) when used on their own. They all rely on being used as part of an EMZ boundary that is as impervious as possible to the passage of surface currents from one side to the other – at least up to its f_{MAX}. Figure 9 shows the main principles of EM zoning.

Combining EM zoning with a single solid (i.e., unsplit) metal reference plane for all return paths, as discussed earlier (see Figures 2 - 8), helps to ensure that all return currents (whether signals, power, DM, CM, stray, etc.) circulate only in their own EMZs, as Figure 10 tries to show.

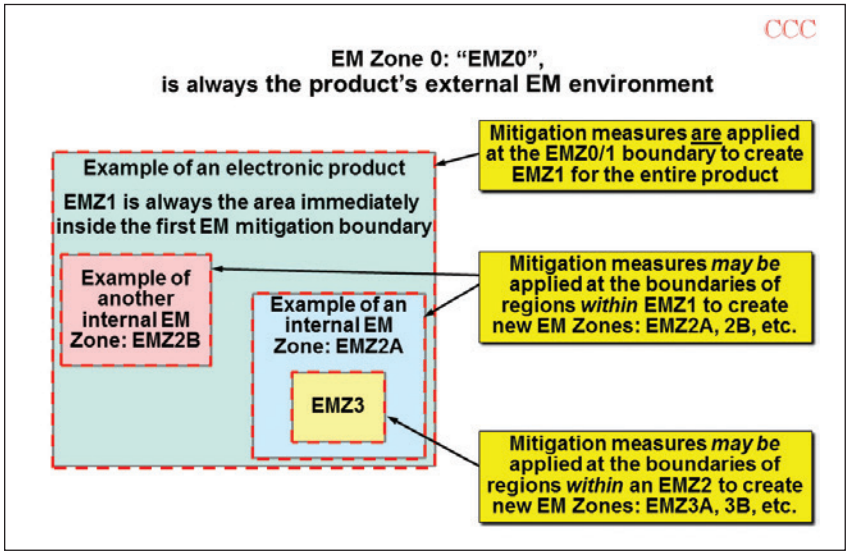


Figure 9: Simple example showing the principles of EM Zoning

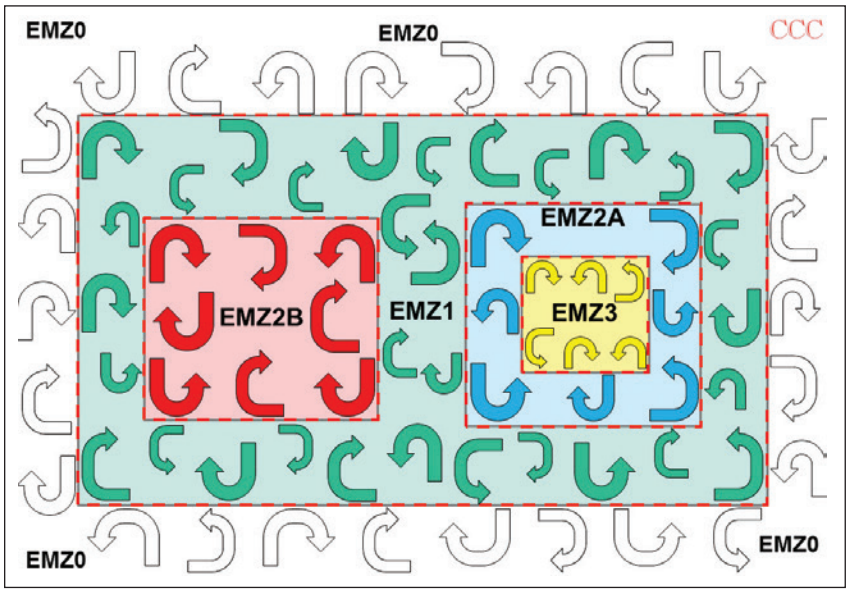


Figure 10: Simple illustration of segregated return currents achieved by using EM Zoning with a single solid, unbroken reference plane for all circuits

Figure 10 attempts to illustrate a most important point for the EMgineering approach, and a very important design technique that, as I said earlier, I have used with 100 percent success since 1981, for SI, PI and EMC. Although the return plane is a single conductor shared by all of the EMZs, the RF currents from one circuit zone *do not spread into other EM zones*. And the absence of splits in the return plane reduces RF resonance problems.

It is common to hear designers making the mistake of believing that RF currents in what they call Ground, Chassis or whatever, will flow throughout its whole conductive structure. This oversimplified Spice-simulator-like approach encourages them to use a great many isolating signal and power converters. As well as not usually being necessary when EM zoning is used with a single reference plane, these converters increase the bill of materials cost and add their own not-insignificant EM noises (see Figures 16 and 18 on page 33) to increase SI, PI and EMC problems.

Understanding…

a. how "skin effect" tends to prevent RF currents from passing from one side of a metal sheet to the other;

b. how return currents "naturally prefer" to flow in the path of least overall impedance, *even if this means flowing through the air instead of a conductor provided for them*; and,

c. how conductors behave as accidental RF antennas,

allows the mechanical design of metal structures, including PCB layers, vehicle chassis, etc., that easily provide excellent SI, PI and EMC with the lowest overall costs.

Spice and other circuit simulators cannot deal with these real, practical design issues (unless we specifically add them in as if they were circuit components). Only field solvers can simulate them accurately.

For good SI, PI and EMC, the design within an EMZ should avoid resonances, and only create inefficient accidental antennas. The design of any EMZ boundary should sufficiently attenuate EM noises that could couple across them, which means that they should also avoid resonances and only have inefficient accidental antenna structures.

EM mitigation techniques must only be applied at an EMZ boundary, in the following order:

1. *Physical Separation*: a gap around a zone boundary, containing no conductors other than the reference plane and the essential interconnections between different EMZs – all of which must be mitigated according to the second technique, below. This reduces the conducted, E, M and EM field coupling ("noise leakage") across the zone boundary. In practice, making EMZs rectangular

helps to maximize the benefits of this technique. Remember – keep the same, solid reference plane throughout. No splits or gaps!

2. *Galvanic Isolation and/or Overvoltage Protection and/or Filtering and/or RF Reference Plane Bonding*, etc., must be applied as necessary to any/every conductor that crosses any zone boundary – *at the very point where it crosses that boundary*.

   "Conductors" mean anything that is electrically conductive, including:

   - PCB traces, wires, cables, etc.;
   - Non-electrical conductors such as fixings, supports, decorative trim, etc.;
   - Conductive liquids (e.g., blood, saline, etc.) even if flowing in non-conductive tubes.

3. *Shielding:* when the physical separation technique above does not sufficiently reduce conducted, E, M or EM field coupling ("noise leakage") across a zone boundary, apply shielding all over the zone's entire volume.

To avoid resonances and to reduce the efficiency of accidental antenna structures, we base our designs on the wavelength, λ, at the highest frequency of concern, f_{MAX}. We also take care to ensure that series impedances are kept low in all signal, data and power conductors, and in all RF bonds; and avoid resonances in circuits, whether the circuit elements responsible are designed-in or due to strays/parasitics.

My EMC design guidelines are based (where appropriate) on the λ at f_{MAX}, which is very cost-effective because it helps prevent both over-engineering and under-engineering. Basing them on the λ at f_{MAX} also future-proofs them against increases in operational, unwanted and tested frequencies. At the time of writing they have been proven in practice to achieve EMC compliance at up to 26GHz on the first prototype, and there is no reason why they should not be equally effective at any higher frequency.

BUT WHAT DO WE MEAN BY f_{MAX}?

f_{MAX} means: the "highest frequency of concern," that is, the highest frequency that needs to be controlled to achieve acceptable SI, PI and EMC for an EMZ and its boundaries with other EMZs. Different EMZs and zone boundaries will usually need to apply different values of f_{MAX} in their design.

How can we determine what f_{MAX} values to apply? Digital devices can emit noise up to 10s of GHz as DM and/or CM from their signal and power pins. CM noise is especially associated with IC ground/power bounce, which is caused by the small but significant impedance between the reference/power distribution networks within an IC, and the reference/power planes in the PCB on which the IC is mounted.

Many designers like to imagine that a "static" input or output is not carrying any broadband noise, but this is never the case for any clocked logic devices. Probing a static pin with a suitably broadband oscilloscope, using a suitably broadband scope probe, will quickly prove this fact.

Most low-frequency analog devices can be susceptible to GHz, perhaps even 10s of GHz, due to the inevitable non-linearities in their semiconductors. Many designers like to imagine that the EM response of an opamp (say) is limited to the linear behavior specified by its data sheets, but it is not. Any exposure to a conducted immunity EMC test up to 80MHz or more, and any exposure to a radiated immunity test up to 1GHz or more, will immediately prove such assumptions to be incorrect.

Power switching devices can emit significant levels of harmonic noise, and experience shows that this can extend to at least 1,000 times their fundamental power switching frequency.

Ideally, we would determine the f_{MAX} characteristics of devices using test methods in the IEC 61967 series (for EM emissions) and in the IEC 62132 series (for EM immunity). A few semiconductor manufacturers are beginning to provide this data, but it will be a long time (if ever) before we will be able to directly compare devices' EMC performance and "maximum frequencies of concern" from their data sheets.

I recommend that electronic design companies equip themselves to perform at least one radiated and one conducted emissions test in the IEC 61967 series, and at least one radiated and one conducted immunity test in the IEC 62132 series. If your company has not yet equipped itself with these tests and made them readily available to all of its designers, my publications and

presentations on close-field probing describe some non-standardized methods for directly identifying a device's f_{MAX} for emissions and immunity, even using D-I-Y probes that take minutes to assemble using low-cost materials that we all have. (See [12] and the 'Choosing Components' part of [11].)

My non-standardized emissions methods are similar to the "surface scan" method of IEC 61967-3 or the magnetic probe method of IEC 61967-6. My non-standardized immunity methods are similar to the bulk current injection (BCI) method in IEC 62132-3 or the direct RF power injection method in IEC 62132-4.

Power converters and modular components (mains power supplies, flat panel displays, motor drives, etc.) can be tested using the regular EMC test methods for emissions and immunity – extending the test frequencies as high as is necessary to be sure that their real f_{MAX} values have been discovered.

We generally find that digital devices have f_{MAX} values for their emissions which are much the same as the f_{MAX} values for their immunity. But this relationship does not hold true for analog devices, or any devices containing any non-digital technologies, which should be immunity tested with frequencies that are either 80 percent amplitude-modulated, or pulse-modulated, with a modulation frequency/rate that is centered within the response range of the intended circuit function. (For example, 1kHz for an audio circuit, 0.5Hz for a typical medical temperature sensor or typical industrial control loop, the exact operating frequency of a solid-state gyroscope (e.g., 14kHz ±50Hz) or any AC-energized sensor or synchro/resolver system.)

Some results of using close-field probing methods briefly described in [12] and [11] to identify devices' f_{MAX}'s for emissions are given in Figures 11-18. In each case I have given the date of the measurement

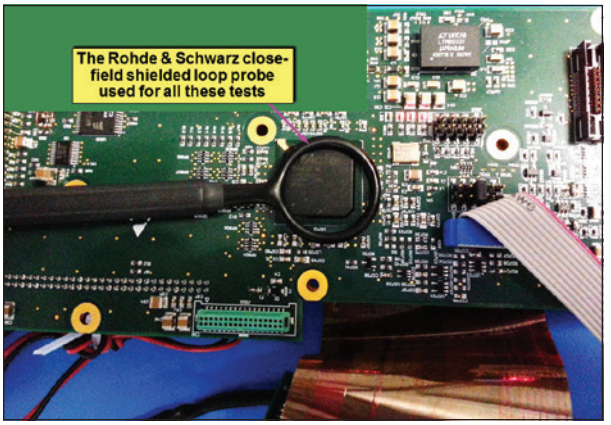


Figure 11: Close-field probing an FPGA and its 112MHz crystal (Actel Pro-Asic A3PE3000, December 2016)

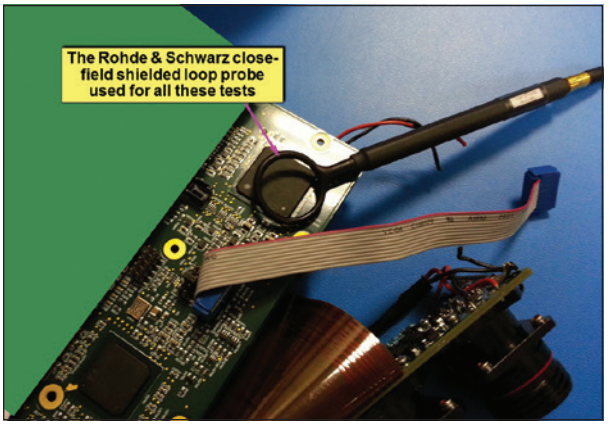


Figure 13: Close-field probing a microprocessor being clocked at 112MHz (Freescale MPC5554, December 2016)

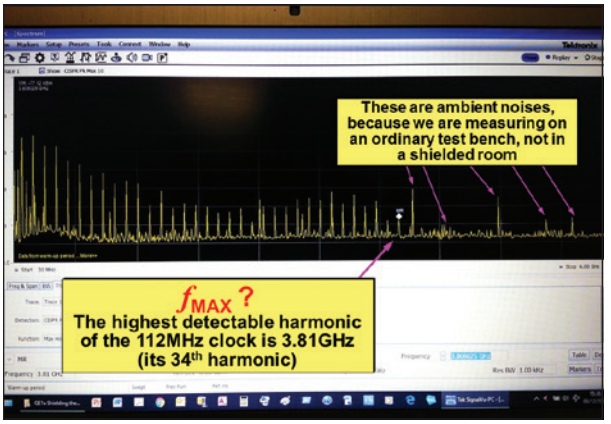


Figure 12: The results of close-field probing the FPGA and its 112MHz crystal (Actel Pro-Asic A3PE3000, December 2016)

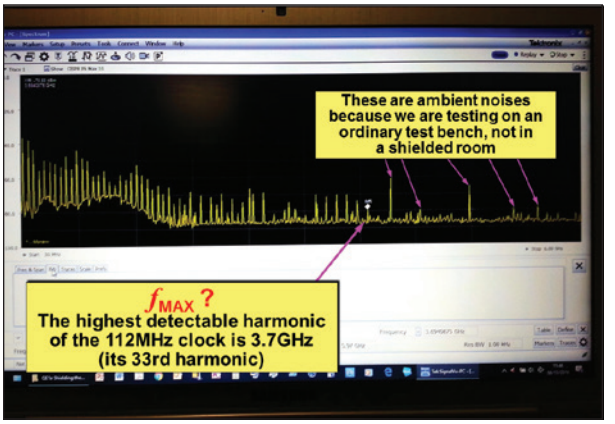


Figure 14: The results of close-field probing the a microprocessor being clocked at 112MHz (Freescale MPC5554, December 2016)

to allow comparisons with similar measurements in future years when the semiconductor dies in all of these devices have been shrunk and their f_{MAX} values are probably higher.

Figures 19 and 20 show the spectra of two common serial communications, 100 and 1000BASE-T Ethernets and three of the various flavors of USB.

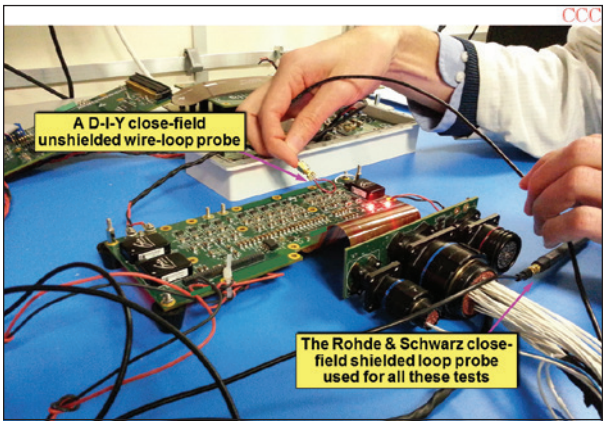


Figure 15: Close-field probing isolating data couplers (Analog Devices 'i-couplers', ADuM12xxx, December 2016)

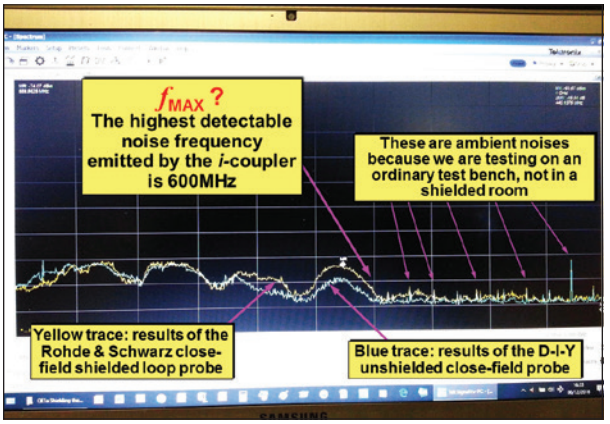


Figure 16: The results of close-field probing the isolating data couplers (Analog Devices 'i-couplers', ADuM12xxx, December 2016)

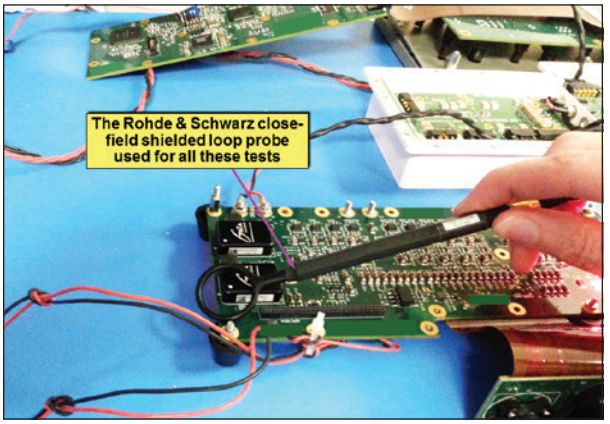


Figure 17: Close-field probing an isolating DC/DC converter (Gaia MGDD series, 5V-output, December 2016)

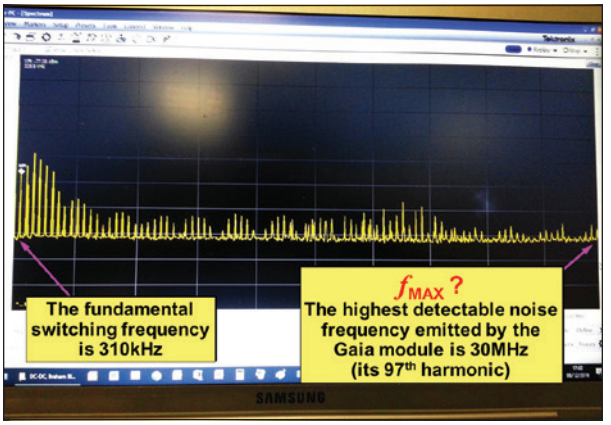


Figure 18: The results of close-field probing the isolating DC/DC converter (Gaia MGDD series, 5V-output, December 2016)

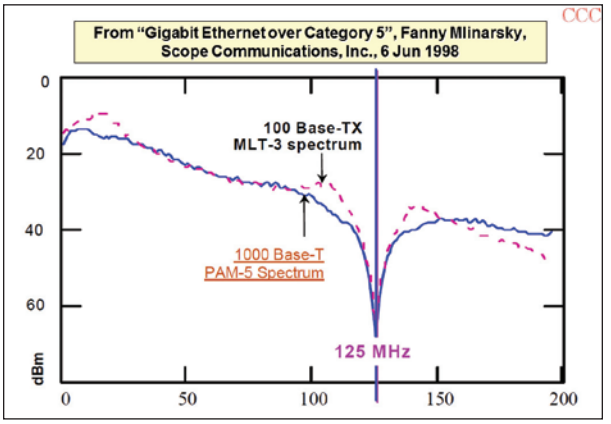


Figure 19: Spectra of 100 and 1000BASE-T Ethernet signals

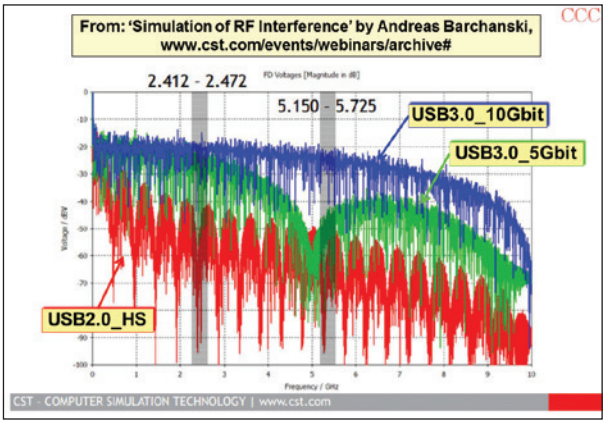


Figure 20: Spectra of three different versions of USB

WHAT f_{MAX} VALUE SHOULD WE USE FOR THE EXTERNAL BOUNDARY: EMZ0/1?

The frequency ranges specified by the relevant emissions/immunity standards are important, but they are based on typical EM environments, which means that about 5-10 percent of EM environments will be worse. But a warranty return rate of 5 or 10 percent is not good, financially, so it is better to meet tougher EMC specifications. Also, EM environments are continually getting worse, whilst EMC test standards are at least 5 years out-of-date when first published, and products need adequate EMC for their whole lifetimes.

Legal compliance with the EU's EMC or Radio Equipment Directives requires not causing or suffering undue amounts of EMI at any frequency, DC-300GHz, regardless of whether a product complies with the relevant test standards. So the best future-proof approach is to make f_{MAX} for the EMZ0/1 boundary the highest frequency that can occur in either the internal devices' maximum emissions/immunity frequencies or in the EM environment. Figures 21 and 22 show two different examples of EM zoning based on f_{MAX}, which I hope are self-explanatory.

WAVELENGTH (λ) – BASED DESIGN GUIDELINES FOR EMZS AND ZONE BOUNDARIES

Having determined the different f_{MAX} values for all of the EMZs and the boundaries between them, and for the external EM environment, we are now able to apply the λ-based design guidelines that I have been describing for the last 15 years or more.

I often say that we measure EMC in MHz (or GHz), and design anti-resonance and anti-antenna structures in meters (or millimeters) respectively, and so my EMC design guidelines contain many guidelines of the type << λ/10 at f_{MAX}, << l/20 at f_{MAX}, and sometimes even < λ/50 at f_{MAX}.

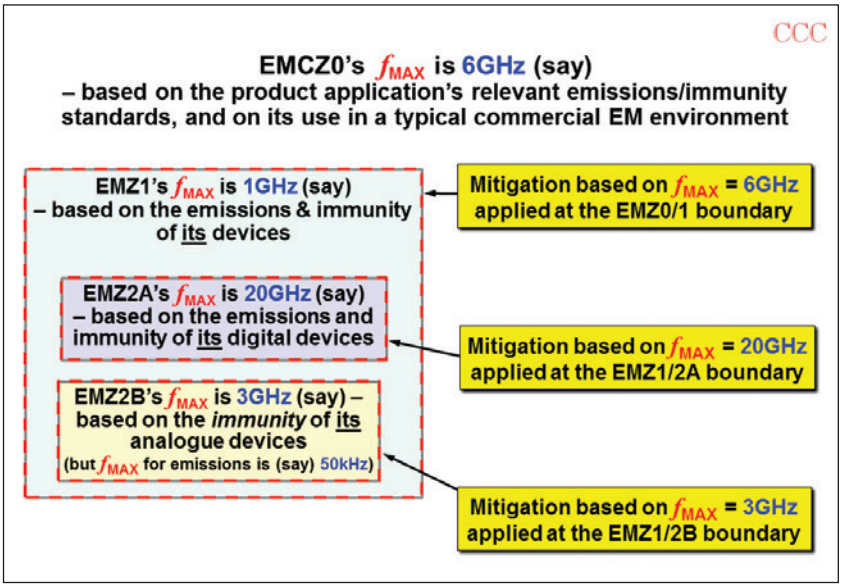


Figure 21: An example of EM Zoning based on f_{MAX}

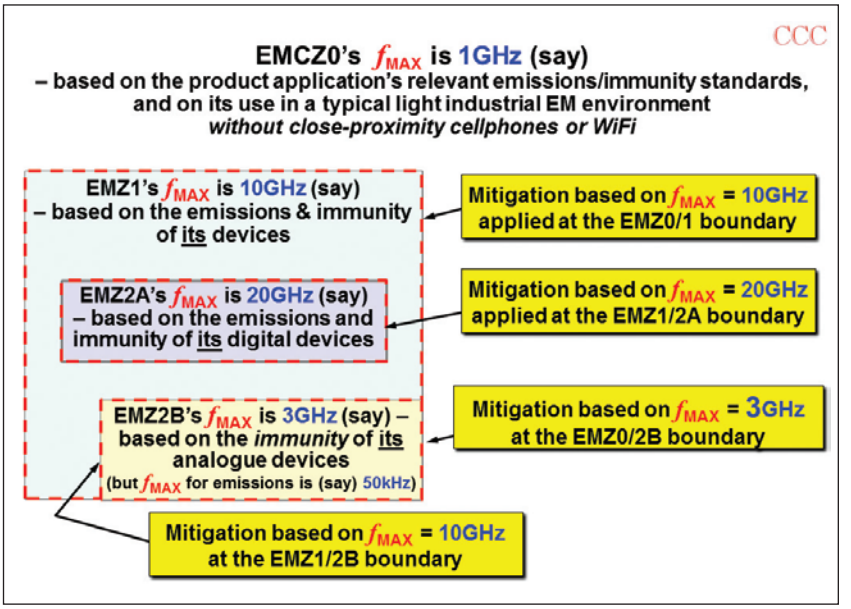


Figure 22: A different example of EM Zoning based on f_{MAX}

CALCULATING THE λ AT f_{MAX}

Frequency (f), wavelength (λ), and the velocity of electromagnetic propagation (v) are related by:

$v = f \cdot \lambda$

In vacuum or air: $v = 3.10^8$ meters/second (well, close enough), so we can say that that $\lambda = 300/f$ (f in MHz gives λ in meters; while f in GHz gives λ in millimeters, mm).

But in PCB traces $v = 3.10^8/\sqrt{\varepsilon_r}$ so we can say that $\lambda_{PCB} = 300/f \cdot \sqrt{\varepsilon_r}$ where ε_r is the relative dielectric constant of the PCB, assumed here to be approximately 4 for FR4 above 1MHz, making both v and λ approximately half what they are in air for a given frequency. So, for FR4 PCBs we generally assume that $\lambda_{PCB} = 150/f$ (as before: f in MHz gives λ in meters; f in GHz gives λ in mm).

λ-BASED DESIGN OF INTERNAL EM ZONES, AND THE BOUNDARIES BETWEEN THEM

Conductor dimensions of λ/10 at f_{MAX} are inefficient accidental antennas. Reducing their dimensions even more, i.e. << λ/10 at f_{MAX}, makes them even more inefficient. Conductors used to provide RF shielding at EMZ boundaries, or as RF Reference structures within an EMZ, make better shields or References the more their gaps or multi-point RF bond spacings are reduced below λ/10 at f_{MAX}.

The f_{MAX} value that guides the design *within* an EMZ should be the highest f_{MAX} for the emissions and immunity of the devices within that zone.

The f_{MAX} value that guides the design of a boundary between internal EMZs should be the highest f_{MAX} for device emissions or immunity of both of the zones on either side of that boundary.

Where at all possible, we should never use any EMZs or conductors with dimensions larger than λ/10 at f_{MAX}. If we have to use such long conductors, we should understand that they need to be treated with care to prevent them from causing or suffering SI, PI or EMC problems.

For example, clock traces on PCBs are often longer than λ/10 at their f_{MAX}. Figures 12 and 14 showed that the f_{MAX} of the 112MHz-clocked devices measured was almost 4GHz, and many modern devices have higher f_{MAX} values than this. In an FR4 PCB: λ/10 at 4GHz is 3.75mm, and since all of the clock traces on the PCB (and many, if not all, of the other traces) are longer than this, they need to either be filtered to reduce their f_{MAX}, or designed using matched transmission-line techniques, both as described in [13] and in my PCB EMC book [4].

Where no more filtering can be applied and neither my << λ/10 at f_{MAX} design guidelines nor matched transmission line techniques can be used, other alternatives include using costly high-specification EM mitigation to contain the very high E and H fields caused by the resulting resonances; and/or dampening the resonances with absorber (if radiated) or resistors (if conducted).

λ-BASED DESIGN OF THE EMZ0/1 BOUNDARY, AND THE INFLUENCE OF EMC STANDARDS

My EMC design guidelines generally assume emissions limits and immunity test levels corresponding to IEC 61000-6-3 and IEC 61000-6-1, which are the "generic" test standards listed under the EMC Directive for the products and equipment intended for use in residential, commercial and light industrial environments.

If applying lower emissions limits than IEC 61000-6-3, we reduce all λ-based guidances accordingly. For example, if having to meet a 10dB lower emissions limit, reduce a λ/10 guideline associated with an EMZ0/1 boundary to λ/30 (because 10dB means a ratio of approximately three).

Likewise, if having to apply higher immunity levels than IEC 61000-6-1, reduce all λ-based guidance accordingly. For example, if the test level is 10 times higher (e.g., 30V/m instead of 3V/m), reduce a λ/20 guideline associated with an EMZ0/1 boundary to λ/200.

However, when an emissions limit or test level is less than those in IEC 61000-6-3 or 61000-6-1 respectively, we should never use any dimensions larger than λ/10 at f_{MAX} (e.g., λ/5) – unless appropriate steps are taken as discussed earlier.

Figures 23 and 24, which I hope are self-explanatory, extend the examples of Figures 21 and 22 to include external cables entering or exiting different EMZs, and the f_{MAX}'s for each cable's shielding (dashed lines) and/or filtering (red rectangles) in each Zone.

λ-BASED DESIGN FOR RF TRANSMITTERS

All the previous λ-based design guidelines have assumed that f_{MAX} is the highest significant frequency in a harmonic spectrum. But RF transmitters are narrowband, and usually very much more powerful than a digital circuit's emissions at even its fundamental clock frequency, never mind its high-order harmonics, so the usual << λ/10 at f_{MAX} guidelines are not appropriate.

Instead, we design transmitters for adequate shielding effectiveness (SE) on a case-by-case basis, as described in my material on shielding and filtering (Chapters 5 and 6 in my EMC Design Techniques book [4], or [14] and [15]). Measuring the antenna's near-fields should allow us to use << λ/10-based design guidelines based on these field strengths compared with IEC 61000-6-1, based on the transmitted frequency instead of the f_{MAX}.

Don't forget that a transmitter's antenna must only extend into EMZ0, and its base must be mounted on the EMZ0/1 boundary to act as its counterpoise. Also, don't overlook the fact that the strong fields emitted by a transmitter's antenna, and the strong surface currents that flow in its counterpoise as a result, will modify the EMZ0 specifications that apply to the entire product or equipment, most likely affecting the design of their EMZ0/1 boundaries too.

It is often the case that a designer will purchase a fully-compliant radio transmitting/receiving module and simply attach it to their product, with its data and power cables plugged into connectors mounted in their product's EMZ0/1 boundary. In this situation, the strong fields emitted by the transmitter module's antenna, and the strong surface currents that flow in its counterpoise as a result, will modify the EMZ0 specifications and the EMZ0/1 boundaries just as described above.

Only if the module is not co-located with the product, for example, is placed far away at the end of a long cable (at least 0.5 meters for a WiFi module or 2 meters for a cellphone module), will it not be likely to affect the EM specifications for the product's EMZ0 or EMZ0/1 boundary. But even then, some additional CM filtering will probably be needed at its connection to the product.

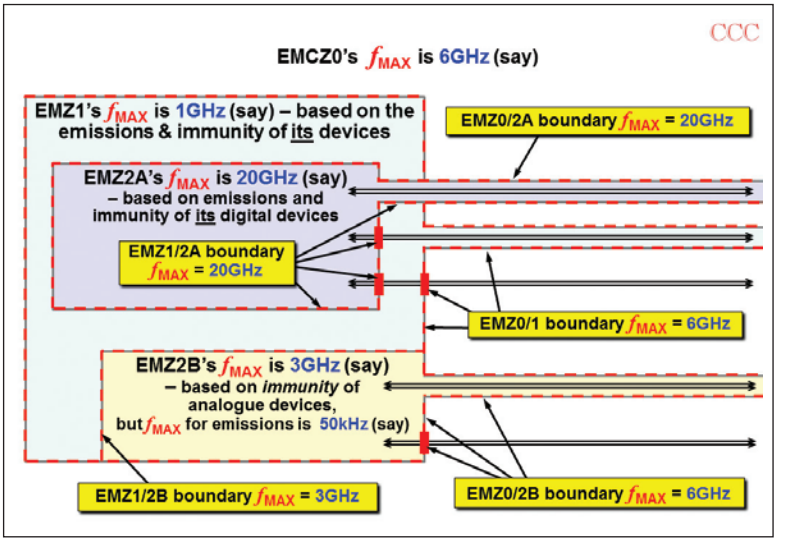


Figure 23: An example of EM Zoning with shielded & unshielded external cables

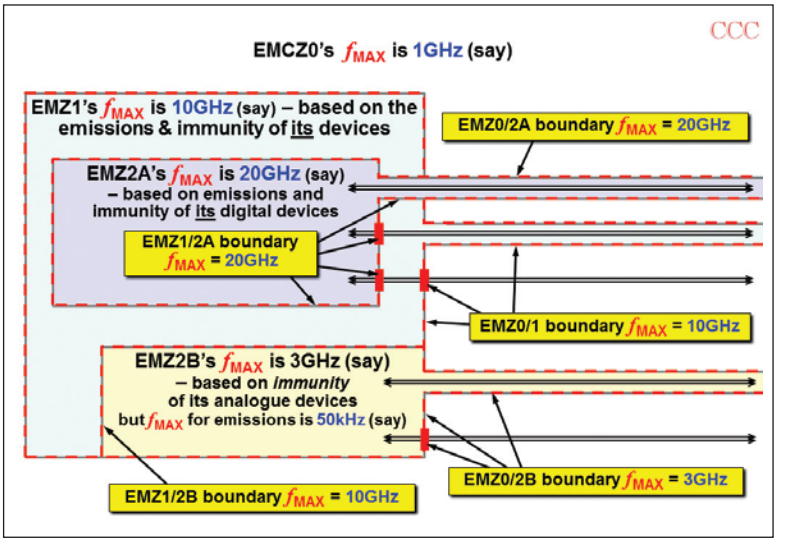


Figure 24: Another example of EM Zoning with shielded & unshielded external cables

CONCLUSIONS

It is now quite reasonable and practical to expect compliance with electromagnetic compatibility requirements to be straightforward, quick, and easy – when using the EMgineering design process that I have introduced in this article. Achieving SI and PI is even easier than achieving EMC, because their requirements are not as tough as good EM engineering, so using the EMgineering design process from the start of a project automatically takes care of them.

ACKNOWLEDGEMENT

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3. My training course notes are available from www.emcstandards.com, and I plan to make all of my training courses available as webinars, on the same site, during 2017.
4. My books on EMC design are available from www.emcacademy.org/books.asp, and are printed on demand. Please note that they are not available (as new copies, anyway) in the English language through Amazon or any other reseller.
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