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Improving the segregation/zoning good design technique for SI, PI and EMC

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Improving the segregation/zoning good design technique for SI, PI and EMC

First published in the EMC Journal, Issue 111, April 2014

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1 Good design techniques are important when starting a project

To meet our signal integrity (SI), power integrity (PI) and electromagnetic compatibility (EMC) specifications quickly, so that we get our new products to market soonest with the lowest overall cost of manufacture, we need good design guidance to know where to start.

Good design guidance helps by reducing the number of design iterations it takes to achieve our functional and regulatory specification, and of course this is most important when we rely on building prototypes and testing them – because each iteration is very time-consuming and also very costly.

For EMC, we can reduce the time and cost of each design iteration by using close-field probing (also known as near-field probing) to investigate prototypes in detail to help ensure that the next iteration deals with all of the EMC problems – insights that are not provided by laboratory testing to the standards required for compliance.

And we can do even better than that by using computer simulators for SI, PI and EMC to provide even more powerful assistance with getting prototypes 'right first time' as quickly as possible.

But even with computer simulators and close-field probing to help analyse our draft designs, it can still take a very long time and/or add much too much cost if we ignore good design practices and just keep analysing, building, probing and testing until we have to freeze a design and start manufacture because otherwise we will miss the market window.

Remember, any iterative approach to anything depends on how close the initial estimate is to the (as yet unknown) final solution. A good initial estimate will iterate to the final solution very quickly indeed, whereas a poor estimate will take several iterations to converge to the same solution.

The more incorrect the initial estimate, the greater the number of iterations required. Sometimes the number of iterations is so large that we run out of time and have to go with what we have got, even though it is not the best solution to the problem.

So, for example, we often find ourselves in EMC test labs, throwing filtering and shielding at a product to make it pass almost regardless of the increase in cost of manufacture, because we just ran out of time. If we don't get the product to market (or to the customer, in the case of custom designs) we lose so many sales (or incur penalty charges) that all the resources consumed to date on the project will be totally wasted.

Even some very large manufacturing companies who have been successful for decades often find themselves in this very difficult situation, which makes one wonder how much better they might have done had they used good design practices from the start of every project.

It is also worth remembering, that in any iterative method, an initial estimate that is too far off the (as yet unknown) solution can result in iterations that do not converge towards the ideal solution, but instead become increasingly worse with each iteration – they diverge instead.

So, even when speeding up the electronic product design process by using computer simulations, not being sufficiently aware of good design practice to start off with a good enough first attempt, can result in a lot of wasted time and effort – and might possibly not even lead to a practicable design solution at all.

2 Good design techniques must continually improve

Like many independent EMC consultants I've been producing good design guidance for years, in articles in this magazine and others, in books and training courses – plus of course for individual designs for specific customers.

However, we have to keep improving these techniques because, as we are all well aware, electronic design is getting more difficult all the time as digital and power conversion speeds continually increase, products continually become more complex, and functional and EMC specifications continually get tougher.

It seems that in this business we have to run just to stand still – but markets and customers are continually demanding shorter design timescales and lower overall costs of manufacture, so even running to stand still is not an option for any company that wants to have a good future – in practice we have to run much faster than that.

Something that I have been thinking about for a while is how to improve the good design guidelines associated with the control of the unwanted radio-frequency voltages and currents that are generated by digital ICs and switch-mode power converters.

3 The challenge of ever-decreasing rise/fall times

The transistors in digital microprocessors and digital signal processors switch at blindingly fast rates, and to do this they have to switch states (1s and 0s) very fast indeed, just a handful of picoseconds is not at all

unusual these days – which Fourier analysis shows us contains a great deal more RF energy at higher frequencies, as Figures 1 and 2 show.

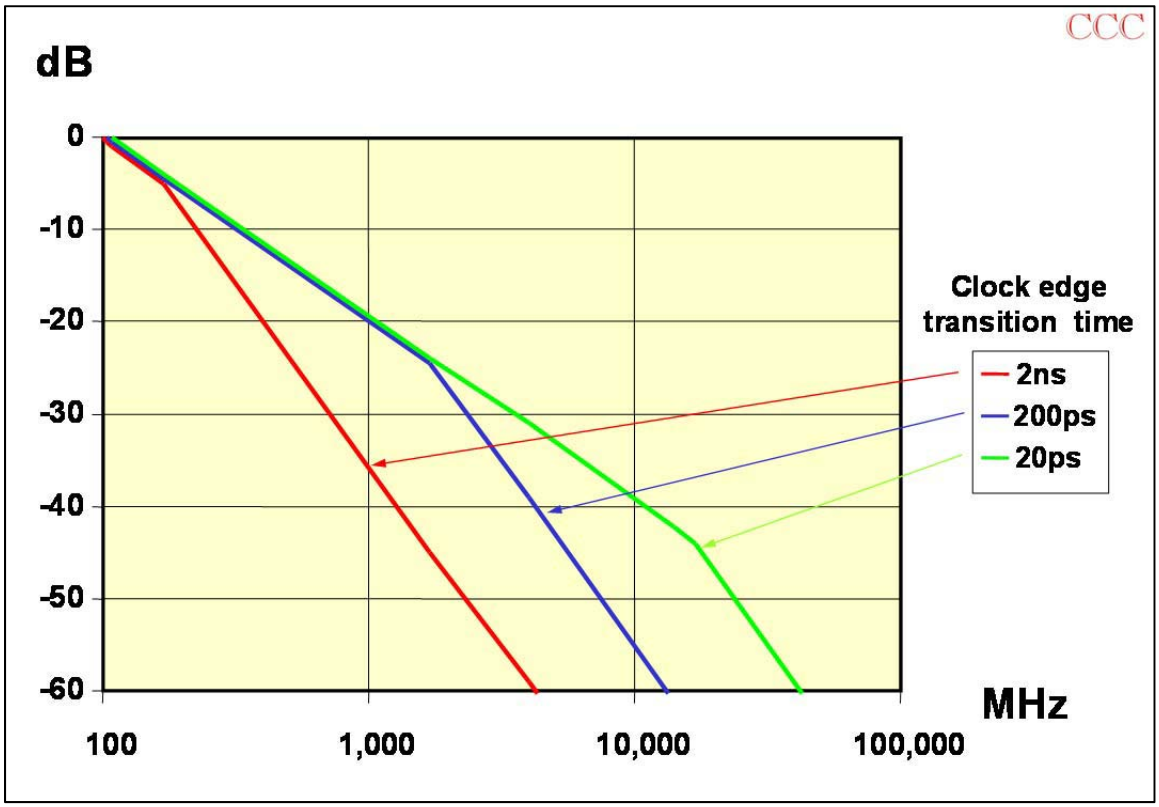

Figure 1 Spectra of 100MHz square-wave with different edge rates

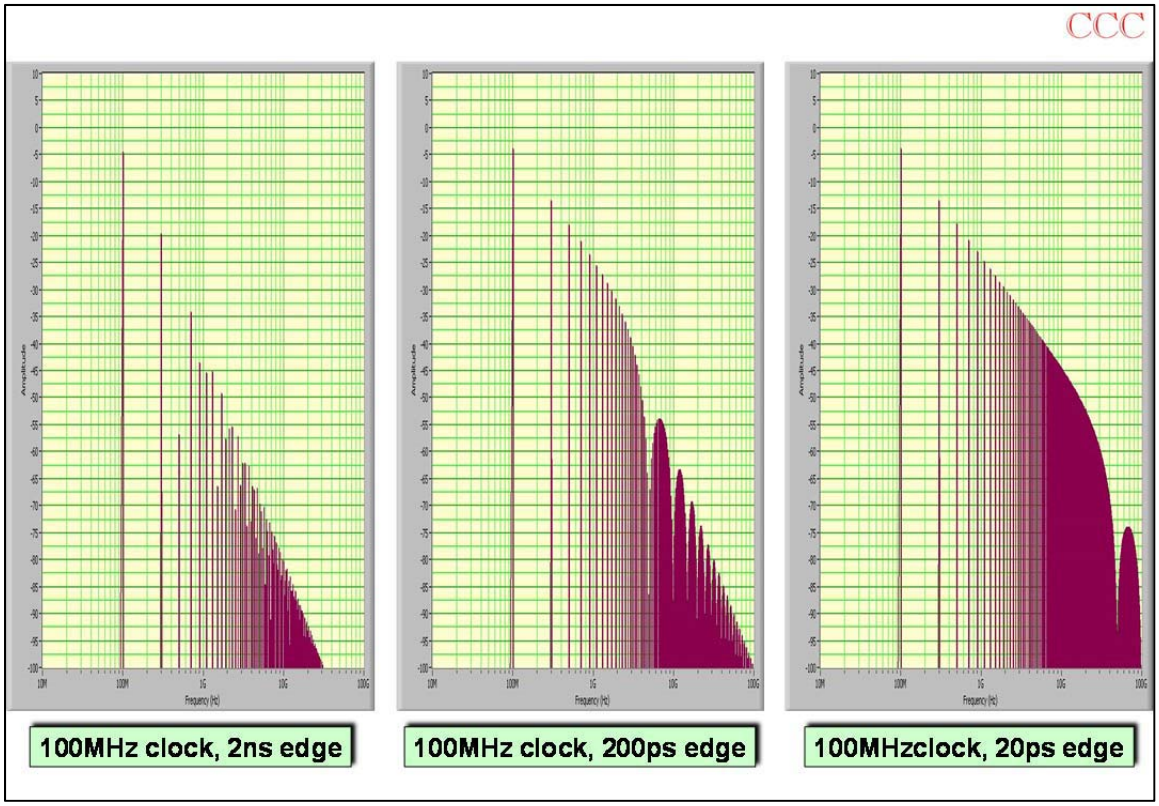

Figure 2 Simulating clock spectra over the range 10MHz – 100GHz
(courtesy of Allan Diamond of Wolfson Microelectronics plc)

Notice that Figures 1 and 2 show the increase in RF content that occurs with increased switching speed (shorter transition times between 0 and 1, and 1 and 0) with a fixed switching frequency of 100MHz, but of course we are also often increasing the switching frequency as well as the switching rate, and Figure 3 shows the effect of this on the clock spectrum.

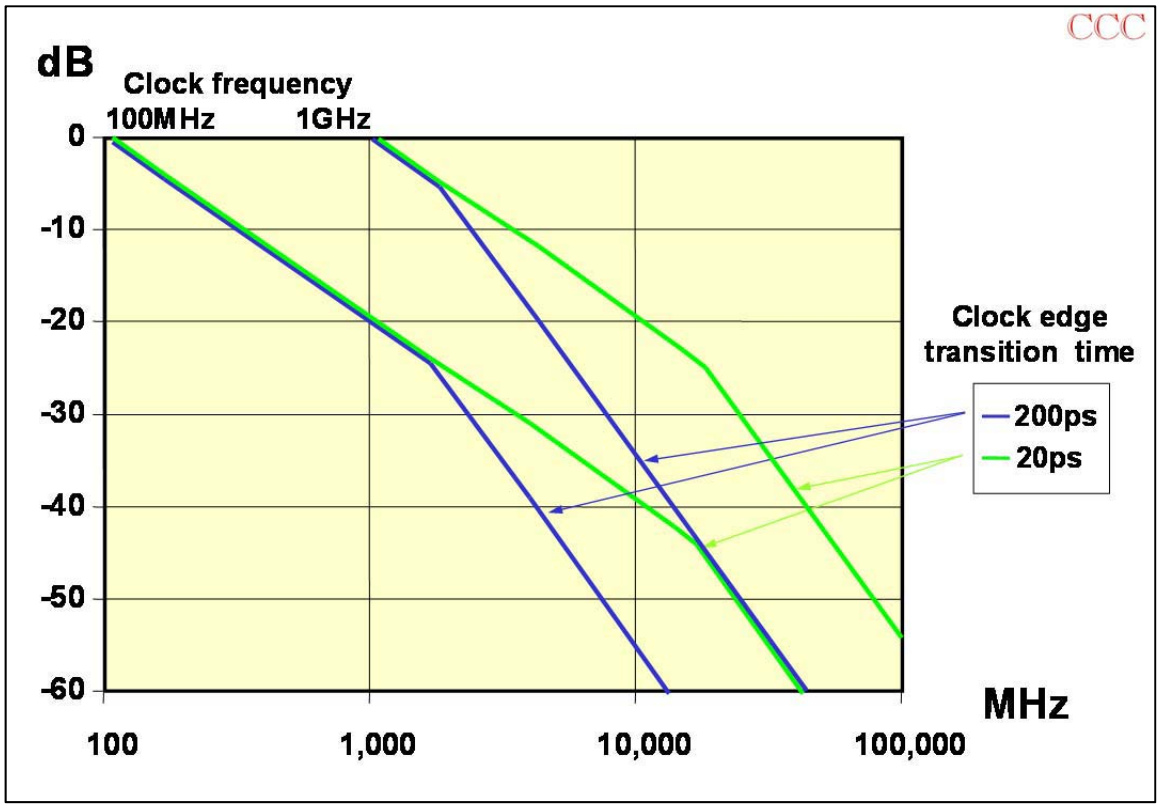

Figure 3 Comparing the spectra of 100MHz and 1GHz square-waves

Switching transistors for use in switch-mode power converters (AC/DC, DC/DC, DC/AC and AC/AC types) are also continually being developed to switch more quickly, to dissipate less heat to reduce size and improve efficiency, and also to permit operation at higher switching frequencies to enable the use of smaller, lighter and less costly inductors, capacitors and transformers.

The current trend is to replace silicon PowerFETs and IGBTs with ones based on silicon carbide (SiC) or Gallium Nitride (GaN) substrates, see [1] [2] [3]. The energy storage in silicon power devices means that they can't switch off instantly, because after their bases or gates terminals have been switched off it takes them quite a while for their stored energy to dissipate and their main current channel to stop conducting.

However, SiC and GaN devices have very much less energy storage in their semiconductors, as shown in Figure 4, and so can switch very much faster than the silicon power devices we are used to. So we will soon be seeing converters of several hundred watts operating at frequencies of 1MHz and above, instead of at a few tens of kHz as they do at the moment, inevitably creating many new challenges for EMC.

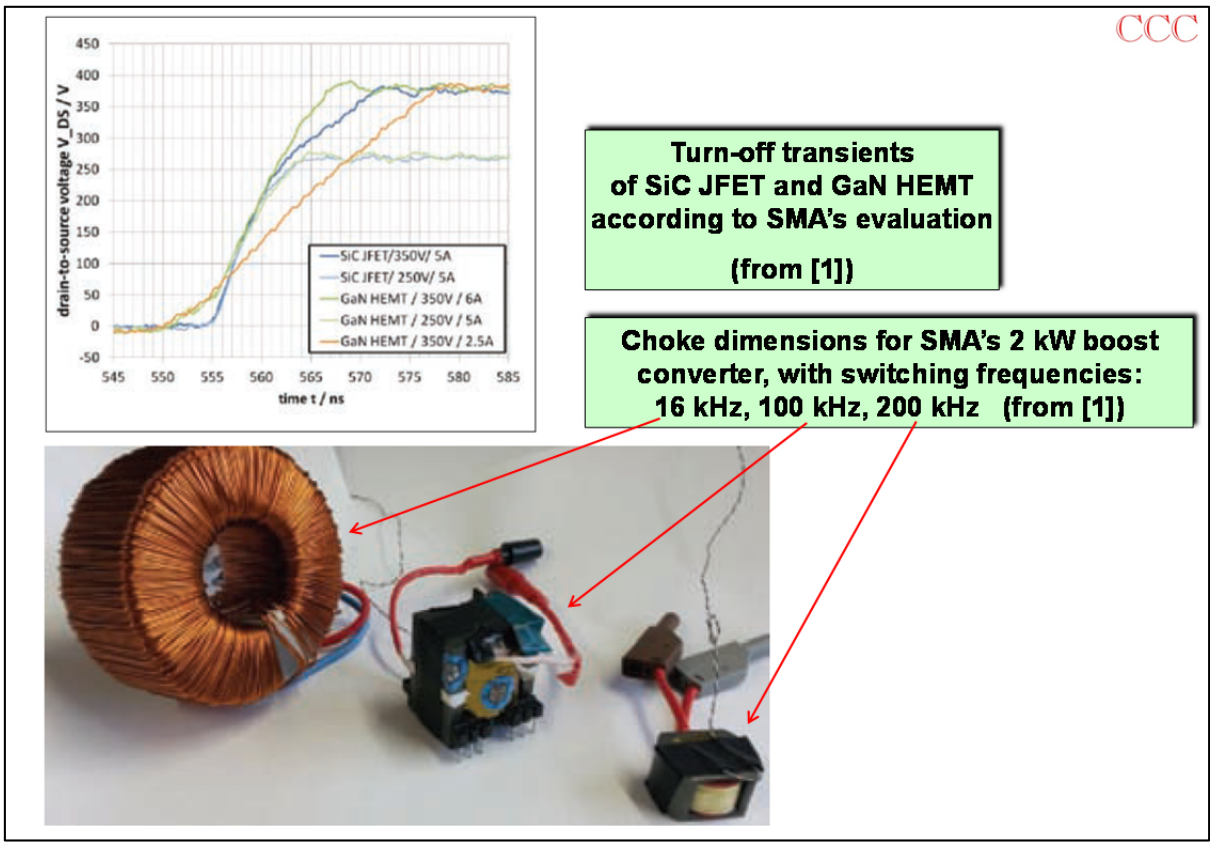

Figure 4 Some benefits of SiC and GaN power devices

But we generally don't need such very high levels of RF in the spectrums of our signals, AC and DC power distribution networks, variable-speed motors, etc. Although such extreme RF content may be necessary for the devices themselves to switch states quickly to achieve their functionality with the smallest size, lowest cost and/or highest efficiency – once it 'escapes' from the devices it is merely RF noise which creates problems for us with SI and/or PI and/or EMC.

Good design guidelines for controlling the RF noise emitted by semiconductor devices has existed for decades, but as switching speeds continually increase the problems of the associated RF noise are continually increasing. The result is that design guidelines also need to continually improve so that the number of iterations we need to quickly produce cost-effective product designs does not increase.

But improving initial design estimates so as to keep pace with digital and switch-mode technologies whilst keeping the number of design iterations the same is actually just 'running fast enough to stand still'. We also need to learn to run faster than this to reduce the number of design iterations, ideally to design 'right first time', to reduce time-to-market whilst also reducing overall-cost-of manufacture.

4 The curse of the 'accidental antennas'

Cost-effectively controlling the unwanted RF noises generated by digital and switch-mode circuits relies on controlling the return paths for their currents so that they do not excite resonances in conductors such as printed circuit board (PCB) traces, components, wires and cables, and conductive structures such as metal housings.

When resonances occur in any of these, they behave as very efficient 'accidental RF antennas' (see Chapters 4.3-4.5 in [4] or Chapters 2.6.3-2.6.4 in [5]). This means that they efficiently convert the RF

currents flowing in them – whether they are wanted differential-mode (DM) currents or unwanted common-mode (CM) stray currents – into radiated RF emissions, which (of course) not what we want.

When we suffer from efficient accidental RF antennas in our electronic products, we need to use filtering and shielding to prevent their RF emissions from causing electromagnetic interference (EMI), especially with radio and TV receivers and other sensitive electronic equipment.

When we look at any 'intentional' RF antenna – we see that it is just a particular arrangement of conductors, or gaps in conductors, carefully design to resonate at one (or more) frequencies for the purposes of specific RF communications or receiving radio or TV broadcasts.

Calling a conductor an antenna, does not endow it with magical radio antenna properties (just like calling a conductor an 'earth' or 'ground' does not magically endow it with the ability to soak up RF noises!). In fact all conductors (even conductive structures that are not used as functional conductors, such as metal support structures) have the characteristics of RF antennas.

Figure 5 shows the 'accidental antenna' characteristics of a 200mm long PCB trace, which because of the dielectric constant of the PCB material (assumed to be FR4) is much the same as it would be for a 400mm long monopole (i.e. whip) antenna.

Figure 6 shows the effect its accidental antenna emissions have on the waveform of a 16MHz square-wave that is passed through it, and Figure 7 shows the resulting spectrum when measured in a test laboratory.

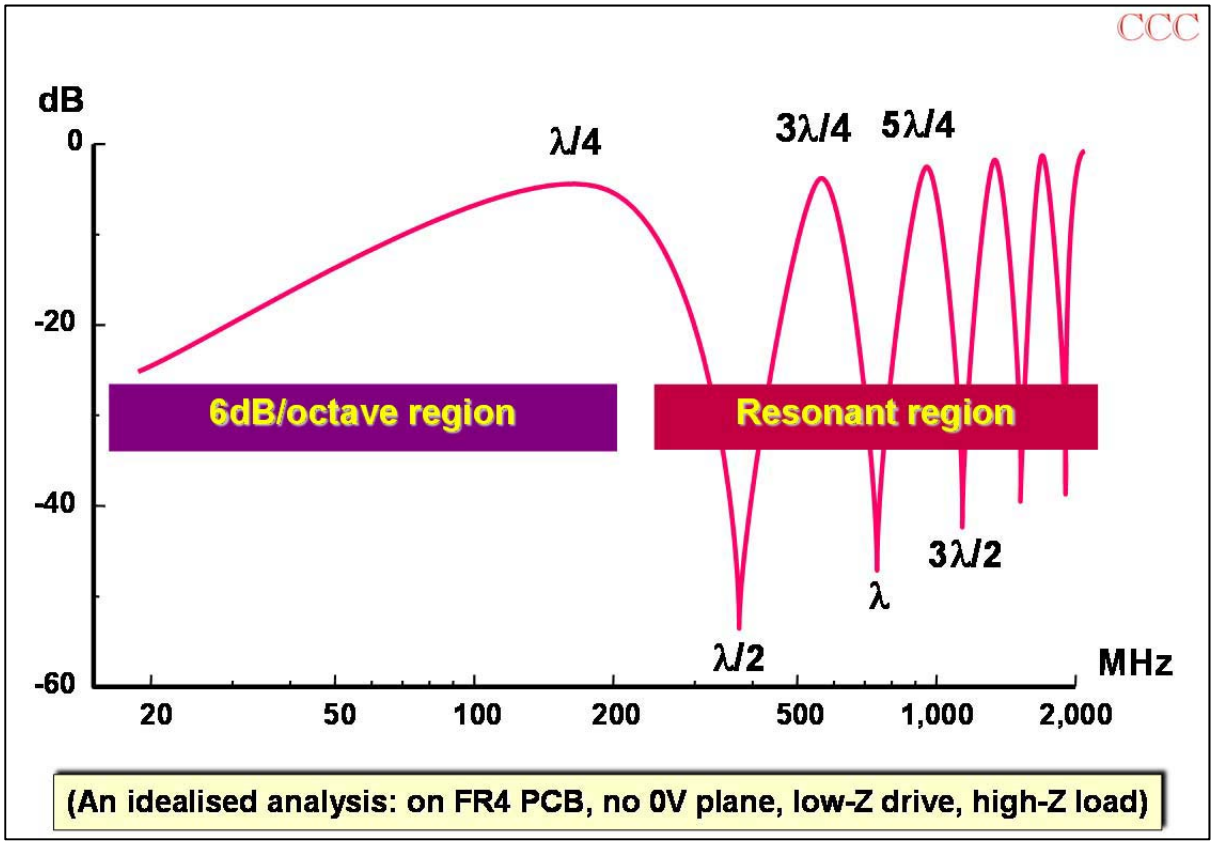

Figure 5 "Antenna efficiency" of a 200 mm PCB trace

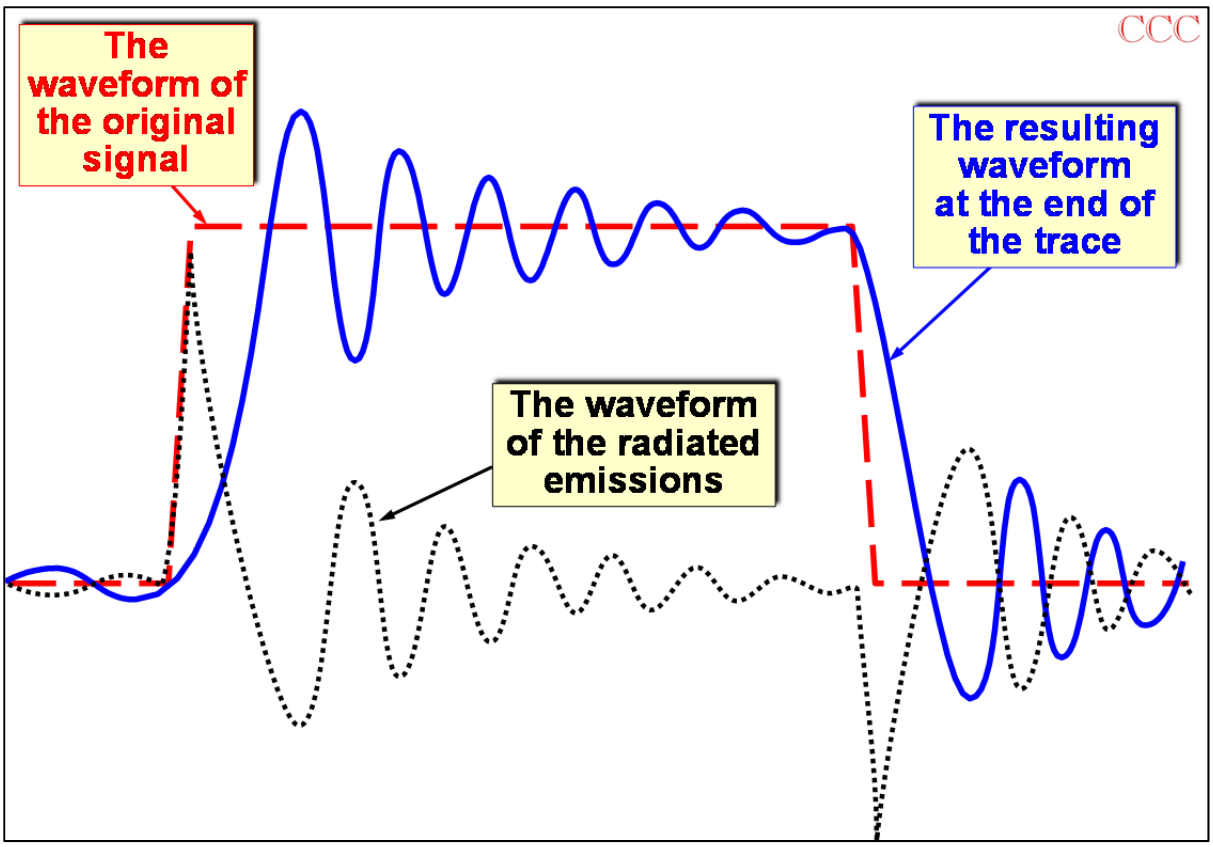

Figure 6 The resulting waveforms after passing along the 200 mm PCB trace

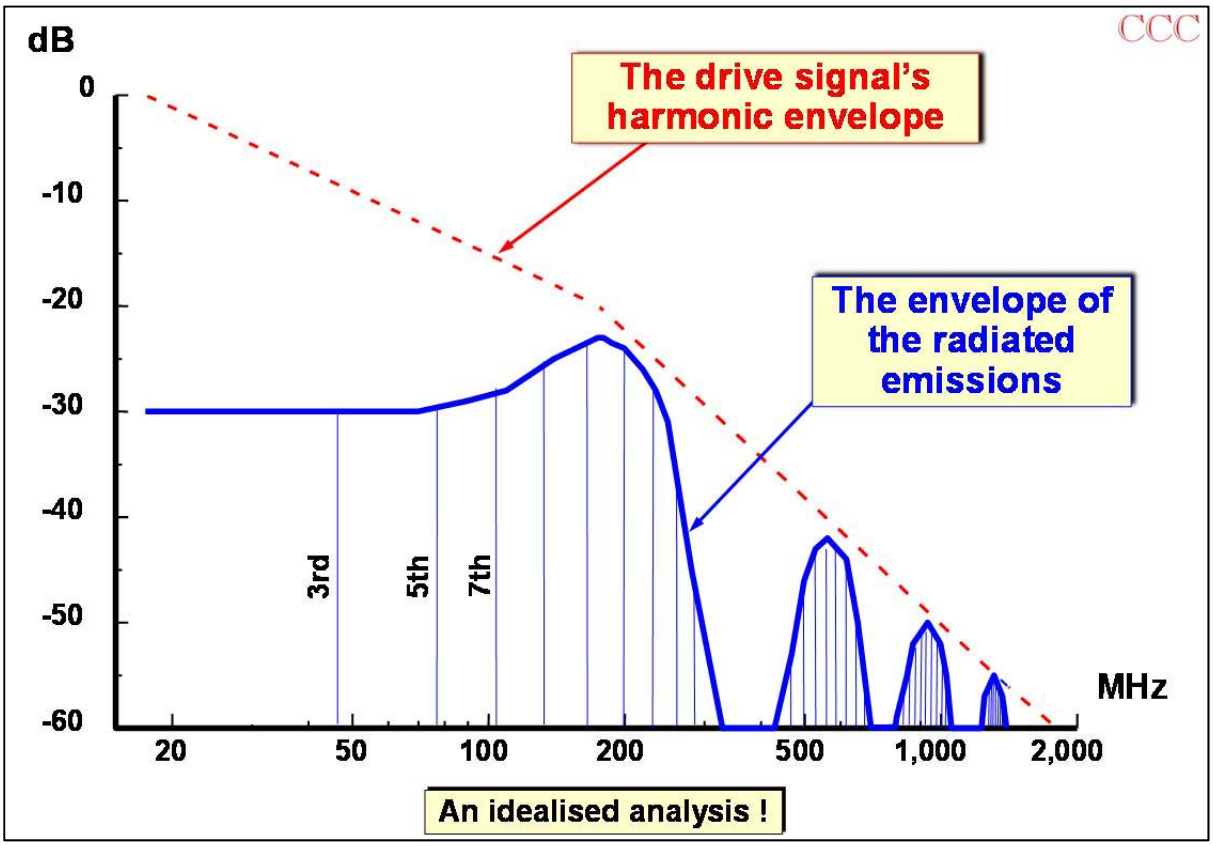

Figure 7 The spectrum of the radiated emissions from the 200mm PCB trace

These figures show the strong relationship between SI and EMC, and why good design for EMC is also good design for SI. It also shows that the waveforms we see on our oscilloscopes have always been telling us about the EMC problems we will discover when our products are tested for compliance to standards.

In this light, good design techniques for SI, PI and EMC can be regarded as 'anti-antenna' techniques – we don't want their RF antenna characteristics, but we are stuck with them so all we can do is make them as ineffective over the frequency range we are concerned with, as we can.

The less efficient we can make the accidental RF antennas in a given electronic design, the lower is the cost, size and weight of the filtering and shielding required to comply with regulatory standards for emissions (i.e. potentially causing EMI) and immunity (i.e. potentially suffering from EMI).

Generally, an electronic design that has too-efficient accidental antennas is also one that is easily interfered with by RF emissions from other electronic equipment, especially *intentional* RF emitters such as licensed radio transmitters and equipment that uses RF energy in the unlicensed ISM bands (e.g. 11.56, 27.12, 40.68 and 915 MHz, 2.45, 5.8 and 24.125 GHz, see IEC 55011). The solution is the same as for excessive emissions – adding filtering and shielding.

It is not generally appreciated that the resonances inherent in filtering and shielding means that relying on higher-specification filtering and shielding to deal with EMC can sometimes make SI and PI significantly worse.

However, using good EMC design techniques to *reduce* the specifications of filtering and shielding (to save cost) will actually *improve* SI and PI, sometimes to a very significant degree.

5 Improving segregation/zoning to reduce accidental antenna effects

Chapter 2 of [5] describes segregation techniques for PCB layout. Similar segregation techniques – sometimes called EMC Zoning – are recommended for the design of products/equipment/systems and installations and are described in Chapters 4.3, 5.3, 6.3, 6.5, and 7.2 of [6]; Chapters 3.3 - 3.6 of [7], and Chapters 4.8 and 5.4 of [8].

In this article I will use the example of good segregation design on a PCB, but the same principles apply to the EMC design of entire products, items of equipment, systems and installations, in all applications.

Figure 8 sketches an example of segregating the circuits on a PCB.

As described in Chapter 2.1 of [5], firstly the 'Outside World' is segregated from the 'Inside World' (but this is not as obvious as it might seem at first, due to the accidental antenna behaviour of unshielded interconnections between the different PCBs in a product).

In the Inside World, the different kinds of circuits (e.g. analogue, RF, switched-mode power conversion, digital, etc.) are segregated physically from each other, and in each case all their components and traces are contained within specified PCB areas, which we could call EMC zones. The Outside and Inside worlds might need to be shielded from each other, and each PCB EMC zone might need to be fitted with a board-level shield (BLS).

Every conductive interconnection between the Outside and Inside worlds might need to be galvanically isolated (e.g. by a transformer or opto-coupler), filtered and/or transient/surge suppressed – as might the conductive interconnections between two PCB EMC zones in the Inside World.

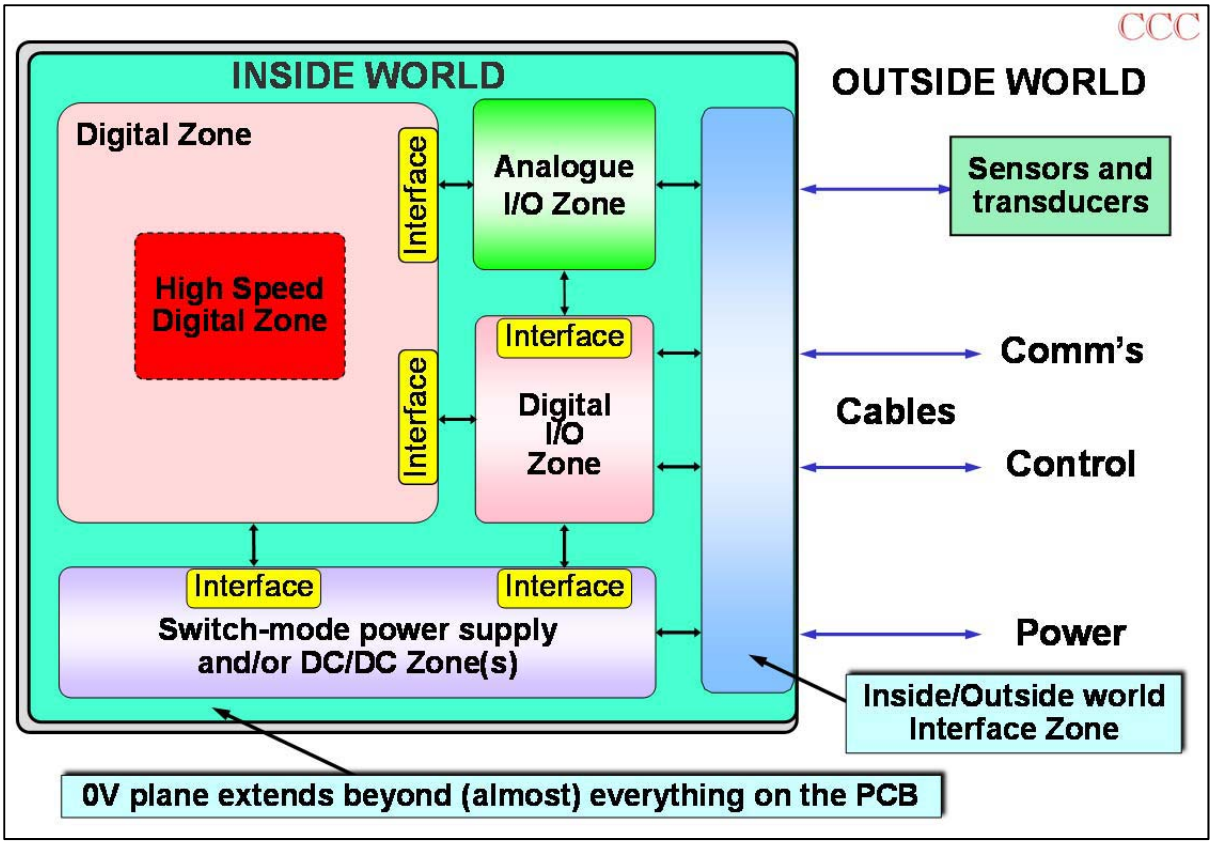

Figure 8 An example of segregating the circuits on a PCB

It is worth mentioning at this point that no pin on any integrated circuit (IC) should ever be permitted to connect directly to any Outside World cable. IC input/output pins connect to the largest transistors on the silicon die, but they are still extremely tiny and so are easily damaged, especially because the designers of some modern ICs using 45nm or less silicon design rules, have decided to leave out the on-chip ESD protection diodes that we have come to expect, and rely upon.

So all IC pins should always be protected by galvanic isolation, filtering and/or transient/surge suppression as necessary, even where the Outside World cables are shielded types (because the cable conductors can be statically charged to quite high levels before they are plugged in).

I find that Common-Mode (CM) chokes are often needed, so usually design them into prototypes, double-padded on the PCB so that individual soft-ferrite RF suppressors, resistors, or zero-Ohm links may be fitted instead if they provide sufficient EMC benefits.

Notice that Figure 8 shows further segregation within EMC zones, and – in particular – the 'Digital zone' has a sub-zone marked 'High-speed zone'.

Until now, I have not written any more about such sub-zoning other than to recommend that it is done where appropriate, and improving this guidance is the subject of this short article.

We could say that almost all good SI, PI and EMC design techniques are actually concerned with anti-antenna design, and the best way of doing this is to make sure that – unless matched transmission-line design is used – all RF currents are returned to their sources with loop current paths that are no longer than one-sixth of a wavelength, i.e. $\lambda/6$ (preferably much less) at the highest frequency of concern: f_{max}.

So, we use decoupling capacitors, filtering and/or shielding to provide all 'send' current paths with 'return' current paths that create small loops within the circuits on our PCB, that noisy, unwanted DM and CM (i.e.

stray) currents will naturally take, so that they do not flow so much in larger loops that make more effective accidental antennas.

(The reason why currents 'prefer' to flow in smaller loops is because they are associated with lower impedances and more compact magnetic and electric fields. Nature (or the laws of physics, if you prefer) always seeks to minimise the energy associated with anything, which is why water droplets always take on the shape that minimises the energy in their surface tension – a tapering shape when falling through the air as rain; a flattened ovoid when stationary on a horizontal surface, a sphere when floating around the International Space Station as simulated in the recent film 'Gravity'.)

(Michael Faraday first noticed that currents always flow in loops, and prefer the loop with the smallest area, way back in the 18th Century – hence 'Faraday's Law of Electromagnetic Induction', one of Maxwell's famous four equations. For more on this topic, refer to [9], [11], [10] or [4].)

(And yes, I know that it is not really the case that a 'send' current flows right around a loop to return to its course – in fact the send and its antiphase return current leave the source at the same instant, flow around the loop and meet up at the opposite side. But it is easier for a circuit designer to think in terms of a current loop.)

At frequencies for which the overall path length around the loop in which we *intend* the noisy RF currents to flow is half a wavelength long, i.e. $\lambda/2$, there is complete inversion of the signal, making it impossible for the current to return in that loop. Such a loop suffers from a resonance of its dimensions, has infinite impedance (is an open-circuit) – even though to our eyes it might look like a very low resistance conductor – so the noisy RF currents will flow in one or more different paths, see Figure 9.

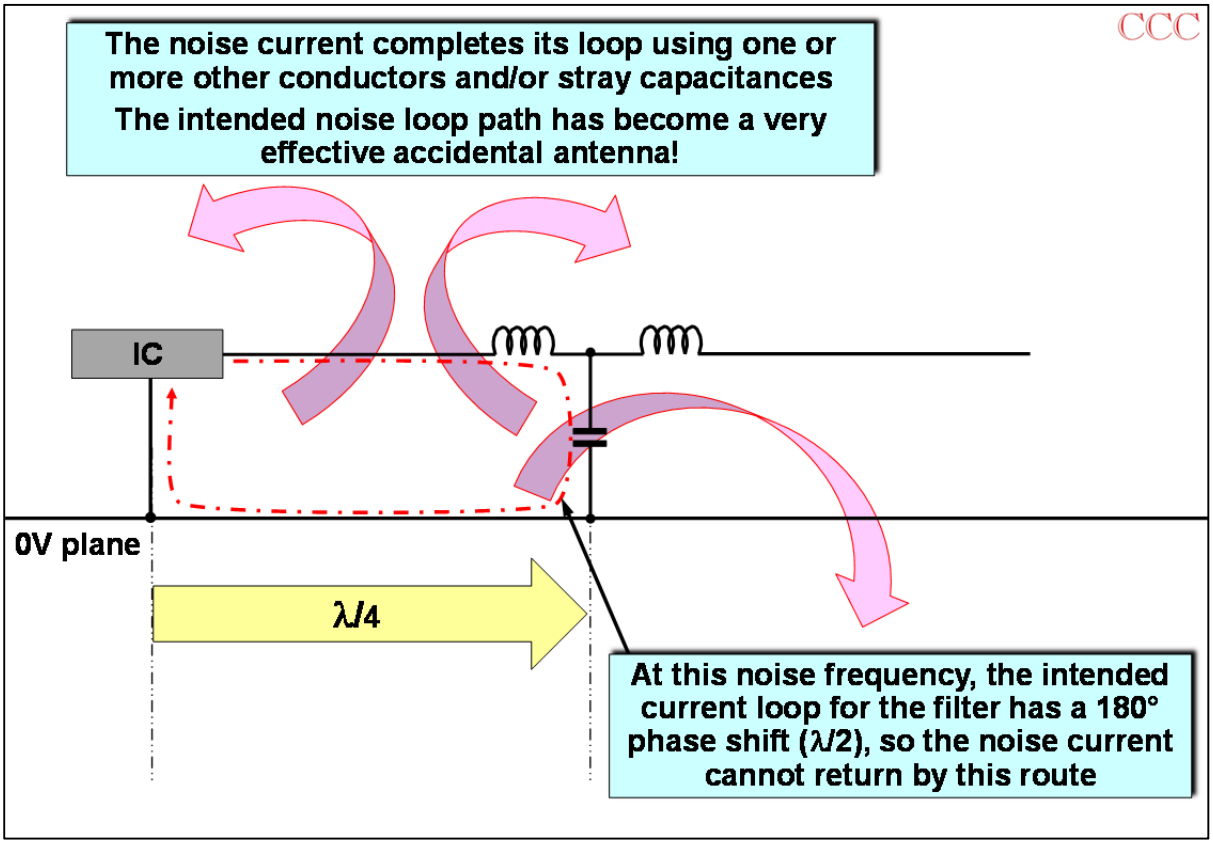

Figure 9 Example of a filter becoming an accidental antenna

Most/all of the noisy RF energy that we intended to recirculate very locally will then flow widely, because the intended path has become a resonant accidental antenna with high efficiency, making our EMC compliance more difficult and more costly.

We must not lose sight of the fact that the actual wavelength at a given frequency depends on the velocity factor associated with dielectrics other than air or vacuum. In air or vacuum, we can assume that the velocity is $3 \cdot 10^8$ metres/sec, so λ in metres = $300/f$ when the frequency is expressed in MHz (GHz gives us λ in millimetres).

But when electric or magnetic fields propagate in a dielectric, the velocity is divided by the square root of the dielectric's constant, ε_r. So, for example, the fields associated with current flow in PCB traces where the board material is FR4 (ε_r = 4.3 between 1MHz and 1GHz) may be assumed to have a velocity of $1.44 \cdot 10^8$ metres/sec, let's say $1.5 \cdot 10^8$ metres/sec to make life easier. With a little less than half the velocity, the wavelength for a given frequency in a PCB is a little less than half of what it is in air or vacuum.

In practice, providing good local return paths for the unwanted RF noise currents generated by our ICs and power-switching transistors, means creating sub-zones that contain ICs or transistors with decoupling capacitors, filters and/or shields that 'shunt' these noise currents into their RF Reference.

The RF Reference for a circuit on a PCB is a 'solid', continuous 0V plane that lies under – and extends beyond – all of a zone's components, pads and traces (see Chapter 4 of [6]).

All of these capacitors, filters or shields must be no further away than $\lambda/12$ at f_{max} from the noise sources they are to control, and preferably much closer. In the case of low-profile decouplers or filters attached directly to traces on the PCB, we can assume that the total loop length is then $\lambda/6$ – the maximum we permit.

But shields are always higher than the components they enclose, and their height adds significantly to the loop length so we must take it into account. However, shield currents have air or vacuum as their dielectric, instead of FR4, so their velocity factor is 100%.

For example, if f_{max} is 1GHz, a total loop length of $\lambda/6$ means that decouplers and filter must be mounted less than $\lambda/12$ away – in FR4 – from the semiconductors that create the RF noise. $\lambda/12$ in FR4 at 1GHz corresponds to a distance of about 12mm.

But this 12mm includes the metallisation of the silicon die, the bond wires and leadframe that connect the die to the PCB traces, plus the length of those traces. Assuming the RF noise is generated in the centre of a die means that the decouplers and filters for an IC that is 20mm square should be located within 2mm of its periphery.

However, if a decoupler or filter is located 36mm from the centre of the IC, the total loop length for the noisy currents they are trying to prevent 'leaking' out will be 72mm – $\lambda/2$ at the f_{max} of 1GHz.

Where the return path for noisy RF currents is provided by a shield, the part of the loop from the semiconductor to the shield, and along the shield back to the RF Reference in the air has a velocity of $3 \cdot 10^8$ metres/sec, and if we set the maximum length of the loop in the PCB to $\lambda/12$ at 1GHz this gives us a radius of 12mm, as before, which corresponds to 24mm of loop length along the shield.

As Figure 11 shows, this means we can have a shield up to 6.5mm tall – although a lower profile will always be better.

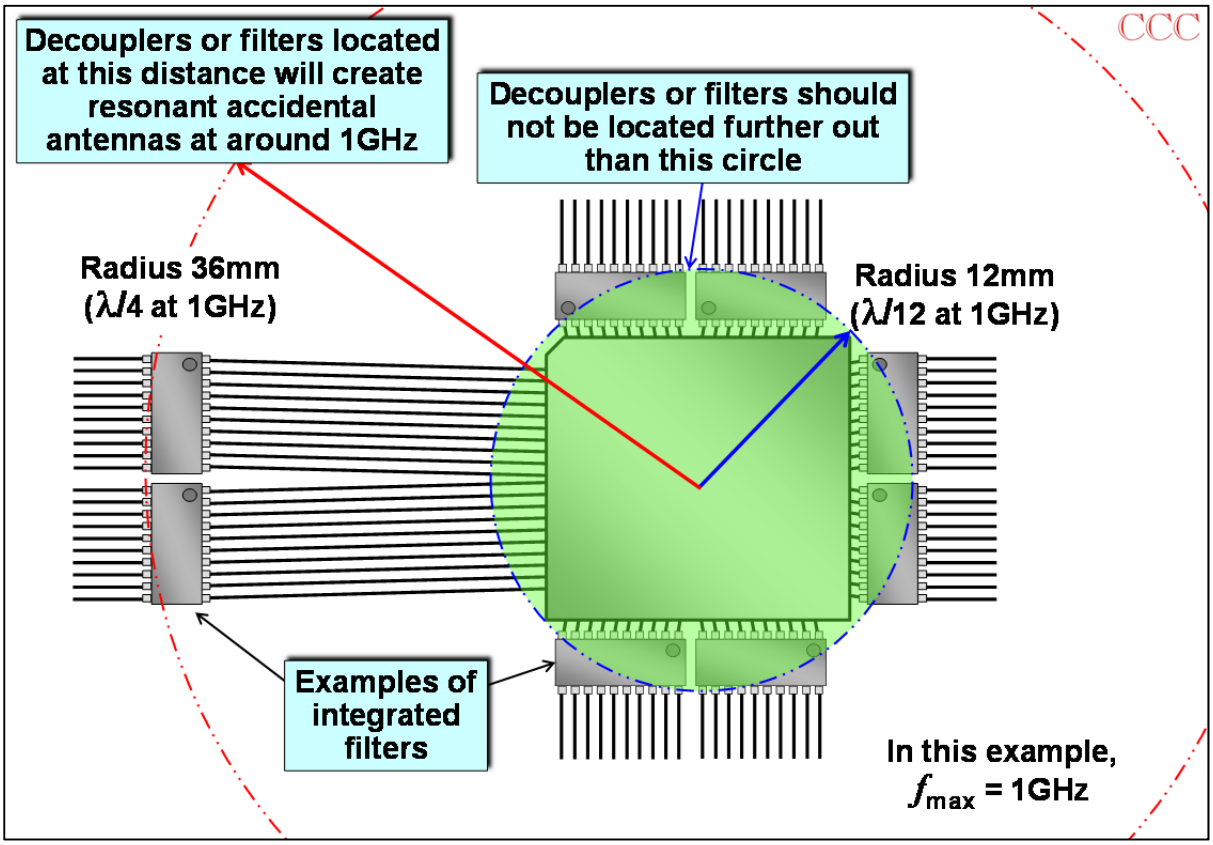

Figure 10 Examples of component layout for good control of current loops

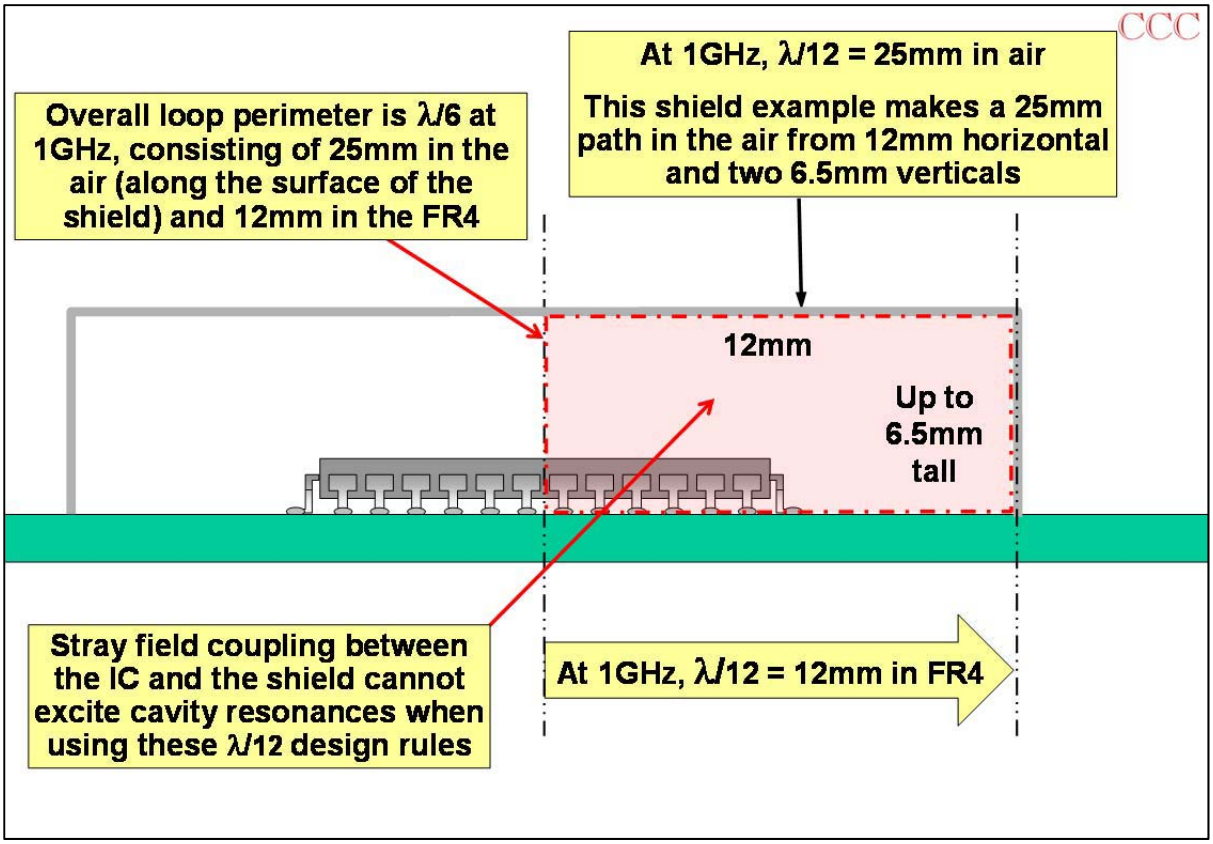

Figure 11 Cross-section view of an IC within a small shield

If we can't return the noisy RF currents generated by our semiconductors back to their sources in the semiconductors with loop path lengths of no greater than $\lambda/6$ overall, we will start to have very significant accidental antenna characteristics including half-wave resonances that can easily increase emissions by at least 20dB, making the RF content of the signal or power spectrum from our ICs much more difficult and costly to suppress.

So we don't have to wait until we have a prototype that we can test in an EMC laboratory, or a computer simulation that captures a PCB assembly in sufficient detail, to discover that we have emissions and/or immunity problems with certain frequencies – we can assess our designs on the basis of whether or not they are preventing RF spectra from exciting resonant accidental antennas in their conductive structures, by using the new 'loop length << $\lambda/6$' design guideline.

6 What is meant by 'the highest frequency of concern', f_{max} ?

f_{max} could be the highest frequency tested by the applicable emissions or immunity standards, but this assumption risks either under or over-engineering.

For example, if the standards test to 3GHz, but our circuits emit significant levels noise at higher frequencies which we do not suppress, we are likely to cause interference and annoy our customers, never mind fail to comply with the EMC Directive because its legal requirements not to cause or suffer undue EMI in normal operation have no frequency restrictions. (Well, OK then, I will admit that it is in fact limited to the range 0Hz to 400GHz).

Where standards test to 3GHz, we are unlikely to see significant energy from our DC/DC converters at anything like this frequency so would risk over-engineering when designing the decoupling, filtering or shielding that returned their noisy currents with loop-lengths << $\lambda/6$.

But we need to take the switched voltage into account when using this design guidance, see below.

Where the semiconductors we use have been tested to IEC 61967 (emissions) and/or IEC 62132 (immunity), and their manufacturers actually makes the test data available to us, we might be able to read f_{max} directly from it.

Otherwise, we can quickly and easily measure it ourselves by using a close-field probe and a spectrum analyser that covers a much higher frequency range than we need simply for complying with the tests. Using manufacturers' evaluation boards, and with the analyser's detector set to Peak mode, we simply hold the probe against the functioning semiconductor, move it around over the surface to maximise the RF noise that is visible, and record f_{max} as being the frequency above which its noise disappears.

Of course, the noise could be below the analyser's noise floor and invisible on this test, and still cause a problem by landing on a resonant frequency in our PCB that selectively amplifies it by 20 or 30dB. To help avoid this possibility, we either set the resolution bandwidth of the analyser to $1/100^{th}$ of that used by the test standard applicable to the product we are designing, or else set the trace averaging to 100 or more. Either way, the measurement becomes much slower so it is best to do it over a limited range of frequencies above the frequency at which the noise disappeared when using the regular RBW.

Also of course, larger close-field probes are more sensitive, so it is best not to use ones that are very small or otherwise very insensitive, whilst avoiding self-resonances in the probes by using them below the frequency their manufacturer specifies them for.

When making our own magnetic close-field probes, we follow the exact same rules as developed above – the loop's perimeter length should be no larger than $\lambda/6$ at the highest frequency we want to measure with it. E-field probes should be no longer than $\lambda/12$. (I generally combine E and H field probes to save time, by making unshielded loop probes.)

7 For switched-mode converters above 3V, use 'loop length << $\lambda/2V$'

We need to be aware that it is the dV/dt and dI/dt that matter when we convert from the time-domain to the frequency domain using the Fourier transform. The rise or fall times will give us the frequency spectrum, but the voltage being switched gives us the amplitude of that spectrum, and the higher the amplitude the worse the emissions – all else being equal.

All my written design guidance so far is based on 3V digital logic, and uses just the rise and fall-time of the digital signals. 23 years of experience in almost all applications shows that it works just fine (after all, it was originally created 33+ years ago to stop microprocessors, which were very new at the time, from interfering with high-performance analogue circuits sharing the same PCB).

Where higher voltages are being switched, it would make good sense to divide the 'loop length << $\lambda/6$' design guideline by the ratio between the switched voltage and 3V, making the guideline maximum loop length $3\lambda/6V$, where V is the switched (peak) voltage.

Of course, we can simply this to $\lambda/2V$, making our new design guideline for switching power converters: 'loop length << $\lambda/2V$'. However, this only applies where the switched voltage is 3V or more, because we risk creating resonant loops for noisy RF currents, if we allow them to be longer than $\lambda/6$.

8 What if the IC's package is larger than $\lambda/6$?

- Use a type of IC package that is smaller than $\lambda/6$ at f_{max}.

  This might mean using die wire-bonded directly onto the PCB (like all LCD displays) or using chip-scale devices (which usually needs microvia board technology too, which can often save cost – see [12]).

- Use embedded capacitors, chokes, etc., laminated within the PCB's structure underneath the body of the too-large IC.

  Embedding PCB components is a rapidly-developing technology, and I might write an article about it soon. An excellent example that is already well-established is embedded (i.e. buried) power decoupling capacitance layers (e.g. Faradflex). For more on embedded PCB components, see [13] and references [26] through [31] in [12].

- Use matched transmission lines (see below).

- Tune the resonances and/or the clock frequency so that no resonances come near any clock harmonics even under worst-case conditions, all the way up to f_{max}.

  I don't usually recommend 'tuning' techniques like this, because they are not very future-proof. When someone else comes to modify our design, and isn't aware that this technique has been

used, they can get very nasty surprises when they go for final EMC testing!
(Experience shows that it is no use expecting other designers to read the notes that the original designer made in the original design documents!)

However, if a given design of product is to be made in very high quantities, and if design control is good, it might well be considered an acceptable risk for the cost it saves.

- Expect the IC to be attached to one or more resonant accidental antennas, and therefore to need high-specification shielding, power supply decoupling, filtering and/or galvanic isolation up to f_{max}.

  A couple of years ago I helped a customer get his product EMC-compliant, despite the fact that it contained a quite large, quite tall, 20W 27GHz fibre-optic laser driver IC. As originally designed, it was way over the emissions limit at 27GHz, but the application of my normal 'wavelength-based' design guidelines was all it took to get him a pass result on the next iteration.

9 Using matched transmission lines

Of course, there is a minimum frequency range needed for communicating the wanted differential-mode (DM) signals from one EMC zone to another on a PCB, or between the Inside and Outside worlds, and where their loop lengths must exceed $\lambda/6$ at f_{max} they should use matched transmission-line design techniques from end-to-end. See Chapter 3.2 of [4], Chapter 6 of [5] and Chapters 2.5.2, 4.7 and 7.6 of [6].

Correctly implemented matched transmission-lines do not resonate, and so do not act as efficient accidental antennas no matter how long they are. However, microstrip lines on PCBs do 'leak' a little of the RF energies they carry, and so it may be necessary to use balanced/differential transmission lines and/or shielding techniques to control this.

10 What's good for emissions is good for SI, PI and immunity too

In the above I have generally discussed the possibilities for improving the 'Segregation' good EMC design technique in the context of EMC radiated emissions, but because it is concerned with the accidental antenna behaviour of printed circuit board (PCB) traces and planes, components, wires and cables, and conductive structures such as metal support structures and housings, the technique is equally effective at improving RF immunity.

And like most good EMC design techniques, it is also a good design technique for SI and PI.

In fact, shielding can be a bad technique for SI and PI, because the resonances that occur in large shielded product enclosures increase the crosstalk between segregated circuit areas. However, the new approach described here, combined with the design rule that no more than one EMC zone is permitted under one BLS, can prevent such crosstalk from happening, and can even improve on the crosstalk that occurs in PCBs with no BLS and no overall shielded enclosure.

11 Conclusion

Well, I've effectively developed this good EMC design technique whilst writing this article to a deadline, so I have no doubt at all that I will need to correct and adjust it in future, most probably in response to the excellent comments I receive from EMC Journal readers!

I intend to write about applying this advanced zoning approach to equipment, systems and installations, in future editions of the EMC Journal.

I hope that this article has prompted some ideas on how to do better SI, PI and EMC design that help us keep pace with the electronics industry, whilst also perhaps reducing the time and cost of EMC compliance.

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