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ESD and Latch Up Damage, Issues with Si-Ge devices

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ESD and Latch-Up Damage – Issues with Si-Ge Devices

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Introduction

Electrostatic discharge (ESD) tests to IEC 61000-4-2 at more than ±4 kilovolts (kV) reliably caused permanent damage to Silicon-Germanium (Si-Ge) integrated circuits (ICs) in a range of microwave wireless datacommunication products.

'Latch-Up' caused by power rail undershoot appeared to be the cause of the problem, and a reliable solution was found.

Neither this failure mode in Si-Ge devices, nor the solution presented here, has – to the author's knowledge – been previously reported.

Si-Ge device technology is at present mostly targeted at microwave wireless applications, which includes the Internet of Things (IOT), and is a candidate for much faster digital processing in the future.

Accordingly, in the near future, Si-Ge may well become a commonplace technology, and significant problems caused by the latch-up failure mode described in this article could become widespread, unless prevented by the use of the techniques described here, or other techniques.

The problem and its solution

A range of battery-powered hand-held microwave radio products used Si-Ge ICs as their Low Noise Amplifier (LNA) radio frequency (RF) amplifiers. At the time, these Si-Ge devices were a relatively new technology, and were used because of their significant noise advantages over earlier (Silicon, Si) ICs.

Unfortunately, the products would not pass personnel electrostatic discharge (ESD) tests to IEC 61000-4-2, at levels higher than ±4kV, because higher ESD voltages reliably destroyed their Si-Ge ICs.

Initially, the RF input pins of the Si-Ge LNA IC were suspected of being the entry point for the damaging ESD transients, but the problem was unchanged when they were linked directly to the IC's 0V (GND) pin by a *very* short wire. This is probably because the device already had integrated overvoltage protection on its input pins (as does, for example, the Si-Ge LNA described by [1]).

After further investigation and some experiments, the conclusion was that the lower band-gap voltage associated with the Germanium (Ge) in the Si-Ge IC was allowing power rail undershoot transients to make them 'Latch Up' (see below), and the resulting power supply overcurrent was causing them to overheat by enough to destroy them.

There are several possible solutions to this problem, but the easiest one to implement throughout the existing range of hand-held microwave radio products in the shortest time, was simply to fit a suitable reverse-biased *power-rated low-forward-voltage* Schottky rectifier across the device's power supply rails, very close to its power (V_{CC}) and 0V (GND) pins.

This modification allowed examples of these products to withstand IEC 61000-4-2 tests at all levels up to ±16kV, the maximum available from the ESD simulator available at that time. Several other modifications were also tried, but had no effect whatsoever on the problem failure mode.

The Si devices on the printed circuit board (PCB) were already well-protected against damage from ESD (including from latch-up), using techniques and devices that have become well-established over recent decades. However, the protection devices used were Si devices, so were clamping undershooting transients on signals and power pins to about 0.7 Volts (V) below the 0V (GND) reference rail.

Clamping at -0.7 V will prevent Si devices from latching up, but the band-gap voltage for Ge transistors is 0.3 V, meaning that latch-up can occur if the clamping does not limit their power rail undershoot to -0.3 V. The existing Si-based transient protection was clearly unable to prevent the SI-Ge transistors in the LNA from latching up.

An appropriate choice of *power-rated low-forward-voltage* Schottky rectifier, connected across the power rails so as to be reverse-biased, prevents power rail undershoots from going more than 0.3V below the 0V (GND) reference, even at the highest level of ESD transient currents that might be coupled. This prevented the Si-Ge transistors in the LNA from latching up at all, see Figure 1.

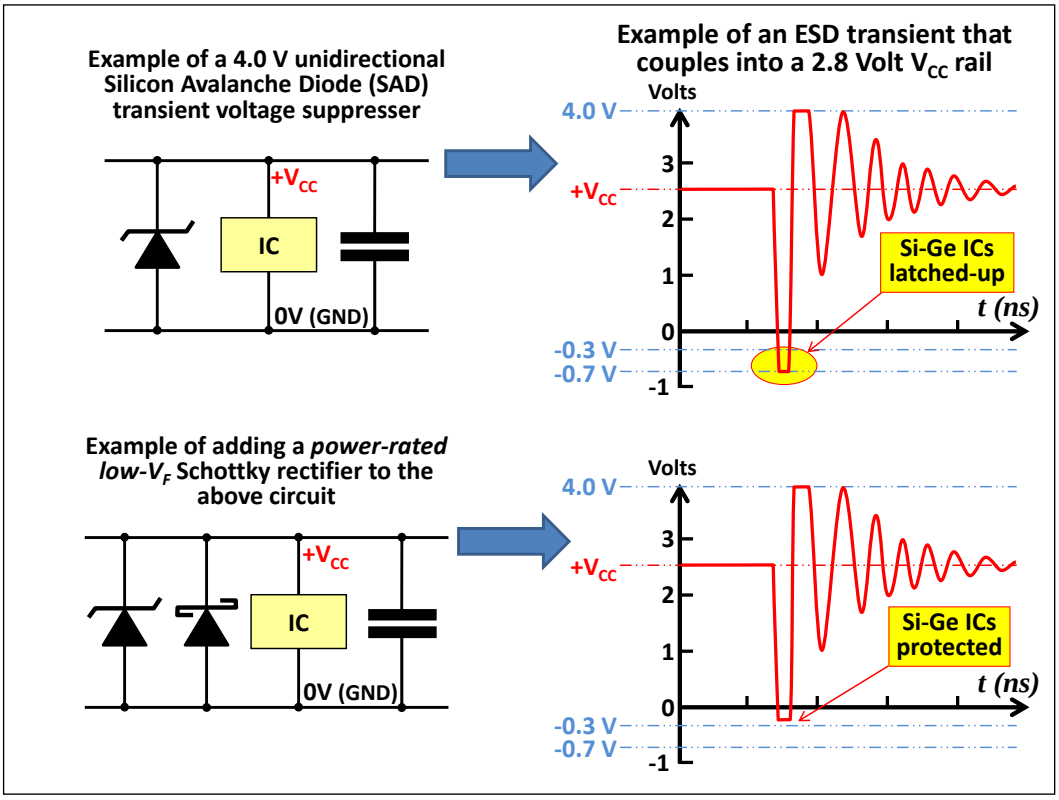

Figure 1 **Comparing Si and Schottky clamping of power rail undershoots**

(Note that this will not be sufficient to protect against electrostatic discharge *directly into* Si-Ge device V_{CC} power rails, but no product design should ever allow this to happen in any case.)

At first sight, a Schottky rectifier should not be able to protect Ge transistors, because the typical forward voltage quoted for Schottky diodes/rectifiers is 0.4 V, which is higher than the 0.3 V latch-up threshold for Ge transistors.

However, all such forward voltages are quoted with respect to some standard forward current, and they are not as precise as implied. The relationship between forward voltage (V_F) and forward current (I_F) in Silicon and Germanium PN junctions, for example, is exponential, whereas in Schottky junctions it is much steeper, as indicated in Figure 2.

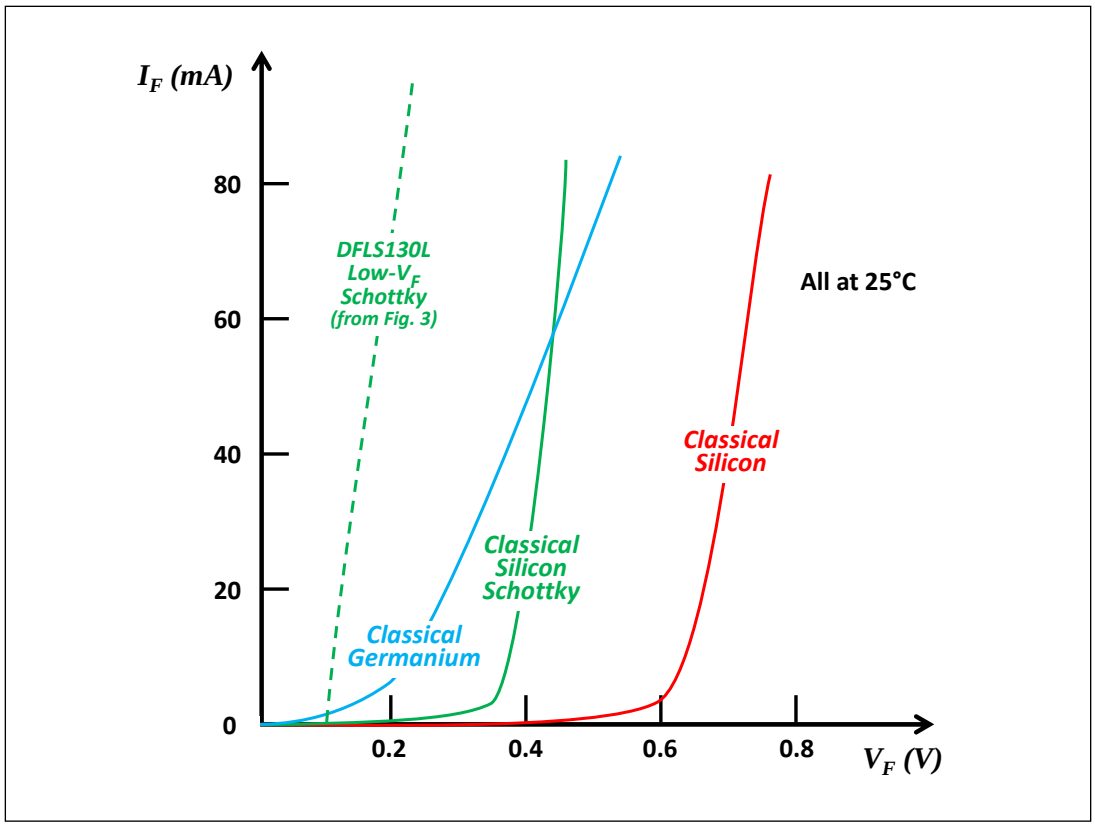

Figure 2 Comparing V_F versus I_F for Ge and Si PN junctions, and Si Schottky junctions

However, Figure 2 is based on generic 'classical' devices that are not representative of all modern semiconductors. There are major variations between the V_F versus I_F curves within each of the device classes, and all such curves are also strongly temperature-dependant.

As an example of modern *power-rated low-V_F* Schottky rectifiers, Figure 3 shows the forward conduction characteristics of the DFLS130L.

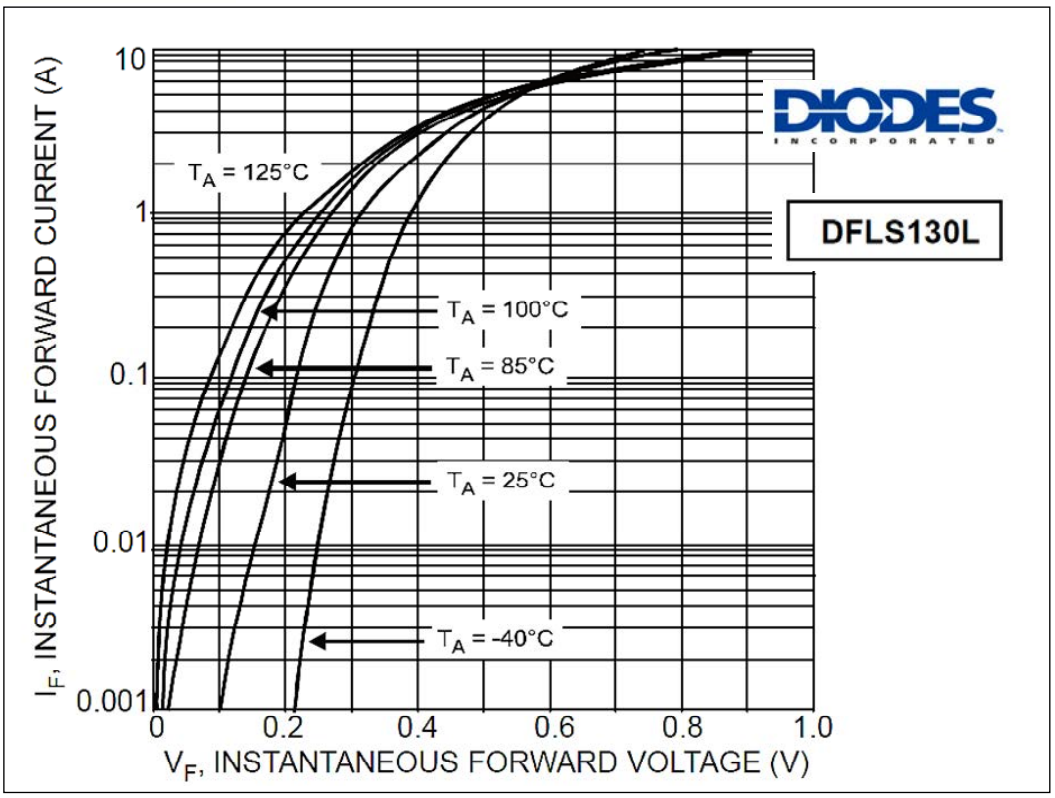

Figure 3 V_F versus I_F for an example modern *power-rated low-V_F* Schottky rectifier

Notice that its V_F versus I_F curves are quite unlike the 'classical' Schottky curves in Figure 2, and that at V_F = 0.3 V – and over -40°C to +175°C – it's typical I_F exceeds 100 mA.

100 mA is a much higher I_F than a classical Ge PN junction at V_F = 0.3 V, and so this Schottky can be expected to be able to be used to protect such Ge devices from latch-ups caused by their power rails undershooting. A portion of the 25°C curve from Figure 3 has been added to Figure 2 to help make this clear.

A complication is that the Si-Ge transistors now being created for RF LNAs and other purposes, may well behave differently from the classical Ge curve in Figure 2. A careful designer will therefore obtain all the V_F versus I_F curves for the *actual Si-Ge ICs to be used*; and compare them with the corresponding V_F versus I_F curves for *power-rated low-V_F* Schottky rectifiers to choose those that provide the greatest protection throughout the intended operational temperature range having regard to their tolerances, costs and sizes.

Introduction to 'Latch-up' in semiconductors

Most ICs are made using the 'dielectric isolation' process, and can therefore suffer damage due to latch-up, which occurs when some combination of temperature, radiation, and electrical transients causes the *parasitic* transistors that this process naturally creates in the IC's silicon bulk (also known as its substrate or dielectric) to turn on.

When an IC is powered correctly these parasitic transistors are reverse-biased (thereby creating the dielectric isolation for which the process is named), and are therefore turned-off. Apart from a small leakage current they have no effect on the functionality of the IC.

But when they are accidentally turned on they make the *intentional* transistors (the ones we purchased the IC for) behave like thyristors that have been turned on ('latched on'). [2] [3] [4] [5] [6] provide much more information on this topic.

Once a thyristor is turned on it has a very low resistance and can carry a great deal of current, which is why they are very useful for switching large amounts of power. They continue to draw current until they are turned off, but the only way to turn them off is to reduce the current flowing through them to a value that is below their 'holding current'.

Thyristors are easy to use for AC mains power control, because they turned off automatically whenever the mains voltage reverses, which it does every 10 ms (for 50Hz supplies) or 8.33 ms (for 60Hz supplies).

However, because ICs are powered from DC voltage supplies, when their *parasitic thyristors* are latched-up the *only* way to get them functioning properly again is to remove their DC power supplies.

The high currents that flow in latched-up ICs cause them to heat up, and if their power supply currents are not limited to safe amounts they can very quickly heat up by enough to suffer fatal damage.

A radioactive particle passing through an IC can lose enough energy into its silicon substrate to turn on these parasitic thyristors. They can also be turned on by the thermal energy created by a sufficiently high temperature. What makes latch-up of interest to EMC designers is that sufficiently reverse-biasing an IC's pin, for example by a transient such as electrostatic discharge (ESD), can *forward* bias its parasitic transistors by enough to cause latch-up. The higher the level of ionising radiation and/or temperature, the lower the transient energy required to cause a latch-up.

For Si ICs, causing latch-up requires a pin to be reverse-biased by around 0.7 V – the band-gap voltage of silicon. So, for example, taking any IC pin more than 0.7 V below its 0V pin (usually marked GND, V_{SS}, V_{EE}, etc.) is almost always a very bad idea, and this should be clear from the maximum and minimum electrical specifications shown for each pin in an IC's data sheets.

However, Ge transistors can be latched-up if any of their pins are reverse-biased by around 0.3 V – the band-gap voltage of Germanium, and this was the cause of the problems experienced by the range of hand-held products that gave rise to this article. Si ICs have benefitted from a continuous programme of improvement over the decades, including improvements in preventing latch-up. Some improvements have addressed the silicon doping processes themselves (for example [7]), and other have integrated active clamps on input and output pins (for example [8]).

Alternative techniques for preventing Ge latch-up due to ESD

Current limiting combined with a 'switch off – wait – switch on' cycle

Limiting the current available from a power rail, for example by foldback, cannot prevent latch-up from occurring, but can prevent devices from overheating by so much that they are damaged.

Please note that in an IC manufactured using the dielectric isolation process, any on-chip over-temperature or overcurrent protection circuits will be defeated, and will not function, during a latch-up.

If the latched-up condition is detected (for example by monitoring the IC's power pin) and a power-off period is enforced (for example by opening an external series-connected FET), the latch-up ceases and the devices have time to cool down before power is re-applied.

If there is insufficient time for the previously latched-up device to cool down sufficiently, its high temperature will immediately cause latch-up to re-establish when the power is re-applied. The more the power supply current is limited as described earlier, the less self-heating occurs in the IC, and the less time it needs to cool down before re-applying the power and reliably resuming full functionality [3].

The same effect can of course be achieved by a manual 'switch off – wait – switch on' cycle, but this is tedious and annoying to users so automatic self-recovery is generally better.

It is important to be aware that in some applications (especially some safety-related applications) permitting latch-up to occur with an automatic (or manual) recovery period, might cause certain risks to be increased by an unacceptable amount – making this approach unsuitable.

Preventing negative excursions of the Si-Ge devices' positive power rail

Design the positive power rail for the Si-Ge devices to have a high-enough storage capacity that is critically-damped at all frequencies up to the highest frequency at which the devices are susceptible to latch-up.

In Si ICs, the parasitic substrate transistors responsible for causing latch-up are generally considered to be slower than the intentionally-designed transistors, but the author does not know if the same applies to the parasitic substrate transistors in Si-Ge ICs. In the absence of any other information, it would be wise to assume that the highest frequency to which a Si-Ge device is susceptible to latch-up is the same as its highest operational frequency (several GHz, and several 10s of GHz in the future).

The aim is to ensure that any transients that can be induced into the positive power rail do not cause a damaging undershoot, either due to charging/discharging of the decoupling/storage capacitors, or due to resonances in the power distribution network (PDN). This approach would prevent the Si-Ge devices from latching up, and so would not require a 'switch off – wait – switch on' cycle at all.

The simplest solution when decoupling an Si-Ge device's power rail is to use an ferrite RF suppresser bead in series – one that has a predominantly resistive impedance from (say) 100MHz to 3GHz (or more), followed by a *single* storage/decoupling capacitor. Special capacitors are available with very low values of equivalent series inductance (ESL), for example [9] [10] [11] [12], specifically for such challenging decoupling applications.

Where two or more capacitors will be used in parallel for decoupling the Si-Ge devices' PDN, resonances will be caused, as shown in Figure 4 and discussed in [13]. These can amplify certain frequency components of the coupled ESD transients, possibly causing power rail undershoots that cause latch-up.

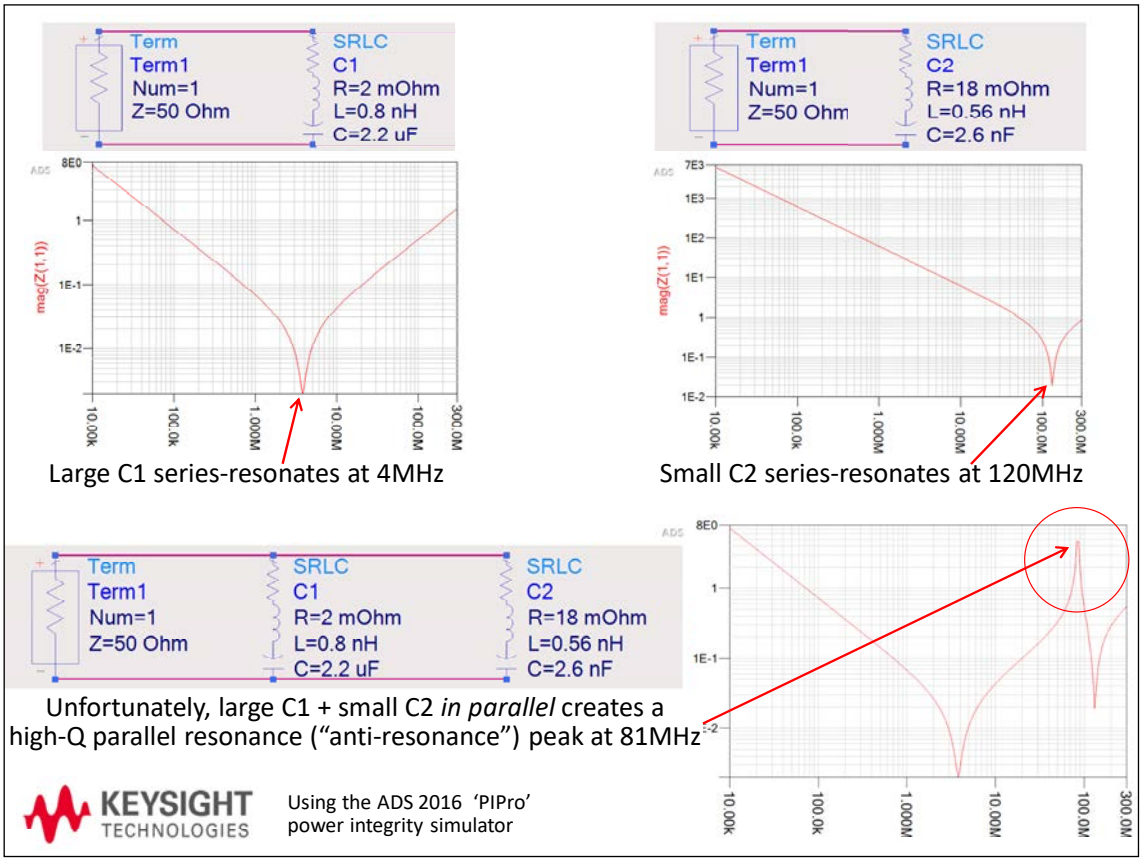

Figure 4 Example of undesirable PDN resonance caused by connecting two different values of capacitor in parallel

The example in Figure 4 used the ADS 2016 'PIPro' power integrity simulator, but any circuit simulator would give the same results for such a simple PDN, using merely 1st-order models for the real capacitors. Careful PDN design, such as that as shown in Figure 5, should be able to reduce the amplitude of PDN resonances sufficiently to prevent Si-Ge latchup due to transient undershoots.

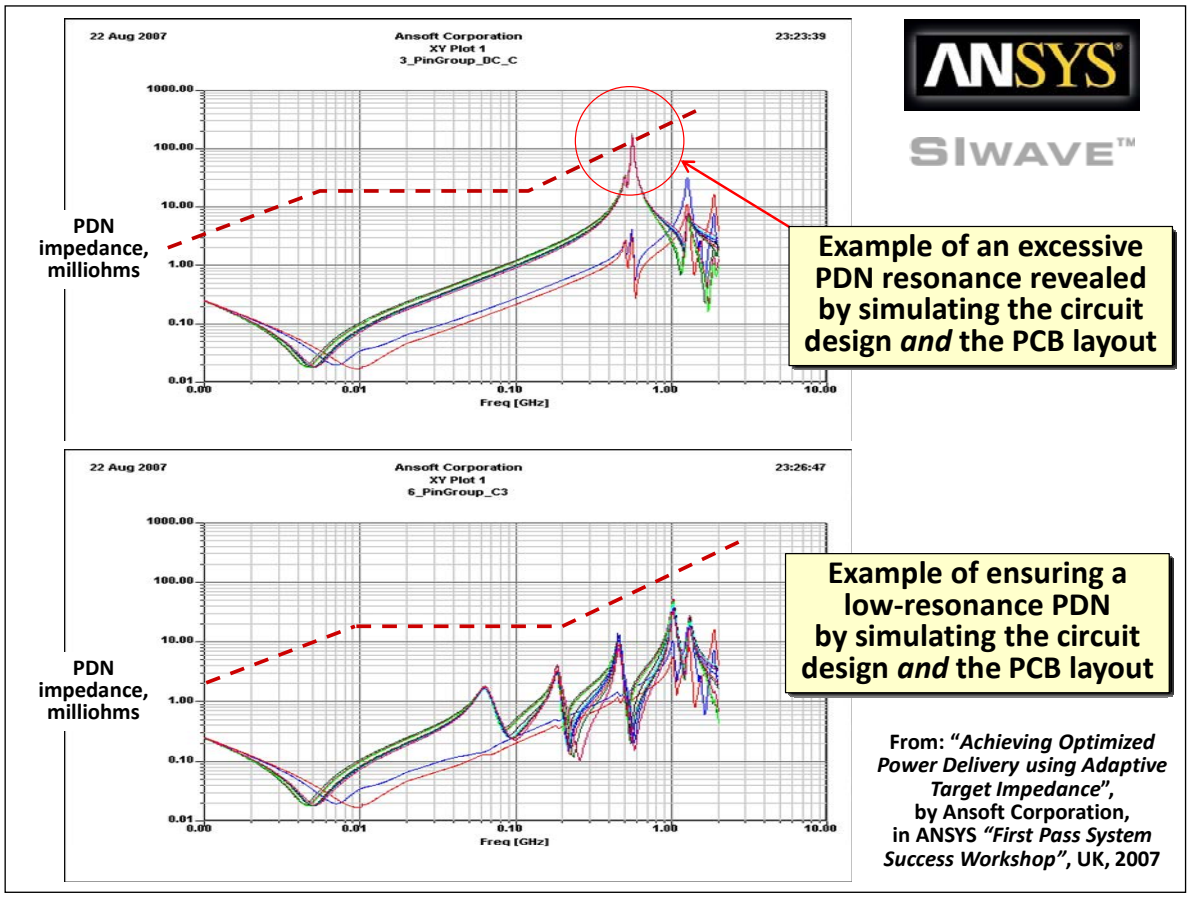

Figure 5 Example of reducing power rail resonances by power integrity simulation

Shielding and filtering

It is tempting to fall back on EMC mitigation techniques such as enclosure shielding and filtering, but these are not always easy to employ successfully (for example on a battery-powered hand-held device). Successful enclosure shielding/filtering solutions also tend to add significant cost and weight.

Shielding a product that has a Liquid-Crystal Display (LCD) and a battery compartment, and making that shielding effective at least up to the highest frequency of operation of a Si-Ge LNA, requires very careful attention to gasketting at all seams and joints to create a sort of 'RF-tight' construction.

And then there is the problem that effectively shielding from directly-injected ESD often requires rather thicker metal shielding than would be desirable in a hand-held device; and of course the shielded window over the LCD cannot use very thick metal without seriously compromising its brightness and readability.

Shielding is generally analysed as providing attenuation ('shielding effectiveness') in the frequency-domain. But transients are usually better described by their time-domain behaviour, and shields analysed from this point of view can be surprisingly ineffective.

RF shields work as the result of the 'Skin Effect' which forces the current density in their bulk metal to decrease by approximately 9 dB for every 'Skin Depth' [14]. For example, the skin depth in pure

copper is approximately $66/\sqrt{f}$ millimetres (mm), where f is the frequency in Hertz. So for example at 1 GHz the skin depth is 0.002 mm (2 µm), at 1 MHz it is 0.066 mm (66 µm), and at 1kHz it is 2 mm.

A 'personnel electrostatic discharge' to a hand-held product (usually when picking it up) is initially a very fast pulse having a very high frequency content, so the transferred electrostatic charge races around the outer skin of the shield at the speed of light, being kept to the outer surface by the very small skin depth at such frequencies. However, once the charge has become uniformly distributed over the outer surface, it becomes a static charge, that is: its frequency is DC, 0 Hz, and skin effect no longer provides any kind of shielding. Eventually, the voltage on the inner surface of the shield will rise to be at the same DC voltage as its outer surface.

We can imagine the charge transferred by the electrostatic event, after its initially rapid distribution over the outer surface of the shield, then 'soaking through' the metal of the shield (like water soaks through paper) and appearing on its inner surface. The thicker the metal, the longer it takes to soak through to the inner surface and the slower the rise-time of the voltage when it appears on the inner surface.

To make a metal shield thick enough so that even a 20 kV discharge to its outer surface appears on its inner surface with a rise-time that is slow enough not to couple potentially damaging currents into signals or power traces on a PCB, obviously depends on the design of the PCB itself. Unless board-level-shields (BLSs) are correctly applied [15] to create two independent layers of shielding, or a single layer of shielding is adequately insulated (see later) so that it cannot experience a direct electrostatic discharge, the circuits to be protected may well require metal shielding that is significantly thicker than a plated metal film, which of course is a problem for any displays.

This situation is worsening with every IC die-shrink, which happens about every two years (according to Moore's Law [16]), increasing the susceptible frequency range of an IC [17] and reducing the amount of transient energy required to cause a latch-up. This means that a product that is shielded sufficiently well to pass its ESD tests, can fail the same tests a couple of years later when assembled with the die-shrunk ICs that will be being manufactured at that time. The author has seen several examples of exactly this happen in real life, when new batches of hand-held products that had been reliable in the past, started to suffer unacceptable rates of customer complaints/returns due to 'locking up' when they were picked up. The only thing that had changed in their design, had been the silicon dies (chips) inside the ICs, which had been replaced by die-shrunk versions.

Unless a 'lifetime buy' of ICs is made when a new product is launched, all products that are in serial manufacture for more than 2 years tend to suffer degraded EMC performance solely due to unavoidable changes in the semiconductor dies used in the manufacture of their ICs. It is quite usual to have to rework a product's design every 5 years or so to maintain sufficient EMC performance for the desired level of customer satisfaction in real operation, simply due to unavoidable IC die shrinks [18] [19].

Insulating the product

Products in plastic housings, with insulated touch-screen controls, can be designed so that they cannot suffer from direct electrostatic discharges. However, indirect discharges (for example, to nearby metalwork) and discharge-free changes in potential from being picked up by someone who is charged up, can still couple transient noise currents into circuits, so some form of shielding will probably still be required.

This shielding can use an overall (enclosure) shield, or BLS, and suitable attention must be paid to the very high frequencies to which Si-Ge devices can be susceptible. However, when direct discharges are prevented by insulation, metal shielding layers need not be as thick as when they must cope with direct discharges.

Usually, LCD and other displays are insulated by 0.5 mm thick plastic films, which will have a typical breakdown voltage of around ±20kV. The actual breakdown voltage will depend on the type of polymer used, its quality of manufacture, and how deeply it can be scratched in use. It is not all that unusual for certain products to need to use thicker polymer films over their displays or controls, for ESD protection, but such thick films can create problems for some types of touchscreens, for the pressure needed to operate controls, and for haptic feedback.

Using special ICs

Most ICs are made by doping patches of a silicon substrate with various chemicals to create N and P regions, which has the side-effect of creating a great number of 'parasitic' transistors within the substrate itself. These are kept turned off by ensuring they experience reversed voltage, so that their only effect is to add a little leakage current. This approach to IC manufacture is called 'dielectric isolation', and if these parasitic substrate transistors ever become sufficiently forward biased, for example by a power or signal undershoot, latch-up or other problems can occur.

However, ICs can be made using either 'trench isolation' or silicon-on-insulator techniques, both of which can totally prevent latch-up. These are more costly IC processes, and so are generally only used to create 'radiation-hardened' or high-temperature ICs for the military and space industries. I don't know if there are any Si-Ge ICs available that use these techniques, as yet.

Problems with the IEC 61000-4-2 ESD test method

The spectrum of ESD 'sparks' is very high indeed, extending to many GHz. Simulating real ESD events (from personnel, furniture, machinery, cables, etc.) is difficult because it is difficult to measure their *real* rise-times in order to create realistic simulators.

This is not a problem as long as the 'ESD gun's' rise-time is faster than the semiconductors can respond to, but this is no longer the case. The 0.7 to 1.0 ns rise-time specified by the current edition of IEC 61000-4-2 has been too slow for modern ICs for some years now, see [20] [21].

This means that products can pass their ESD tests in one laboratory, and fail the same test in a different laboratory that uses a different make of ESD gun. It also means that even when products pass all ESD tests in any test laboratories, they can still suffer from real-life ESD events. As this article has shown, the consequences of such failures can include permanent damage to Si-Ge devices.

[22] shows that these issues are especially important for portable products.

It seems likely from [20] and [21] that many modern Si devices are already susceptible to ESD events of less than 100ns, and will respond to shorter events in the future as the result of further die-shrinks. We may also confidently assume that at any given stage of die-shrinking, Si-Ge devices will respond to even shorter events than plain Si devices.

We have known since 2001 that micro-gap discharges can create ESD events with risetimes of 50ps [23], therefore there clearly needs to be a continuing evolution of ESD guns to provide ever-faster

risetimes so that manufacturers can ensure that their products will not suffer unacceptably high failure rates due to ESD in real-life. Some EMC test equipment suppliers make micro-gap discharge tips for this reason. Although they do not comply with IEC 61000-4-2, they may well help to ensure the reliability of modern products in real life.

Conclusion

Electrostatic discharge (ESD) tests to IEC 61000-4-2 at more than ±4 kilovolts (kV) reliably caused permanent damage to certain Si-Ge ICs, due to latch-up apparently caused by power rail undershoot.

Design techniques that prevent latch-up of Si ICs has become well-established over recent decades, but these techniques do not totally protect Si-Ge devices from potentially destructive latch-ups.

A reliable solution was found for the Si-Ge devices concerned, which relies upon an appropriate choice of *power-rated low-forward-voltage* Schottky rectifiers, and this article has provided sufficient information for designers to protect modern Si-Ge devices against this failure.

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Author's biography

Keith graduated from Imperial College, London, in 1972 with an Honours Degree in Electrical Engineering. He has been a member of the IEE/IET since 1977 and a member of the IEEE since 1997. Appointed IET Fellow and IEEE Senior Member in 2010.

After working as an electronic designer, then as project manager and design department manager, Keith started Cherry Clough Consultants in 1990 to help companies reduce financial risks and project timescales through the use of proven good EMC engineering practices.

Over the last 27 years, Keith has provided design consultancy and training courses to well-over over 800 customers worldwide, presented many papers and published many articles and three books, all on good EMC engineering techniques, and on EMC for Functional Safety. Most of his articles and training courses have recently started to be made available through the new emcstandards.co.uk website.

Keith has chaired the IET's Working Group on EMC and Functional Safety since 1997, and is the UK's appointed expert to the IEC committees on 61000-1-2 (the basic standard on EMC for Functional Safety), 60601-1-2 (risk management of EMC for medical devices), and 61000-6-7 (generic standard on EMC for Functional Safety).

Since 2015 he has also chaired the IEEE Standards P1848 team creating: "IEEE Standard Practice for Techniques and Measures to Manage Functional Safety and Other Risks with Regard to Electromagnetic Disturbances".

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