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EMC and Signal Integrity

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Feature Article

Cover story, March/April Issue, 1999

EMC and Signal Integrity

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As clock speeds increase, electronics designers need ever greater control over signal integrity, but many continue to regard EMC as nothing more than a regulatory burden. This article shows why that view is short-sighted, and suggests an early start for EMC design.

For most electronic equipment, design for signal integrity is taken into account—at least to some extent—in the first PCB iteration. Design for EMC, in contrast, is often postponed until the product is advanced enough to be sent out for EMC testing, by which time it is too late to implement most low-cost time saving measures. Such an ad hoc approach has little to recommend it. Those with EMC experience know well that design for EMC should begin right at the start of any new project, to help develop a competitive product that will get to market on time.

As it happens, the very techniques that are most effective at promoting EMC at the circuit and PCB level are also good means of improving signal integrity. Full application of such techniques, in pursuit of the maximum achievable EMC benefits, often automatically results in excellent signal integrity. When implemented early in a project, this can in turn produce more-robust designs, often eliminating the need for at least one prototype iteration.

I am not going to describe specific EMC techniques here. Instead, I want to explore some of the reasons for the close relationship between EMC and signal integrity. In addition, I'll describe an easy way for designers to predict the EMC performance of prototype hardware using an oscilloscope.

Oscilloscopes versus Spectrum Analyzers

One of the major problems faced by digital designers in addressing EMC consists in the fact that they routinely work in the time domain. Their usual tools are oscilloscopes, pattern generators, logic analyzers, and the like, all of which measure or create voltage signals on the basis of time (hence the time base of an oscilloscope).

EMC engineers, by contrast, operate in the frequency domain, using spectrum analyzers, which measure variances in signal voltages on the basis of frequency. (I am including EMC receivers in the category of spectrum analyzers.)

Thus, we may note that the horizontal axis (x-axis) of an oscilloscope is marked in units of time (e.g., 2 ns/div), whereas that of a spectrum analyzer is marked in units of frequency (e.g., 10 MHz/div). The ability to visualize digital signals, or the interference they emit, in both the time and frequency domains (i.e., waveforms and spectra) can be very useful indeed, and can often provide significant insight into how to optimize designs for signal integrity as well as EMC. Having a good understanding of both domains feels quite satisfying intellectually—and what's more, it can help you beat the pants off the competition.

Signals Are Waves; PCB Traces Are Waveguides

The underlying physical reality of electrical signals and how they get from place to place can be properly described only by quantum electrodynamics (QED), but even though QED is the most accurate scientific theory ever devised, nobody understands exactly why it works the way it does.

Instead, let's use Maxwell's ideas about electromagnetic wave propagation. These tell us that an electrical signal is really an electromagnetic wave that may be guided by arrangements of conductors or dielectrics. This means that all of our conductors (e.g., silicon metallization masks, bond wires, IC lead frames, PCB traces, connectors, wires, cables, metalwork, etc.) are actually waveguides. To simplify the concept even further, we might say that every signal has an associated current, which always flows in a closed loop (remember Kirchhoff's law?).

Historically, most designers have considered only the "send" part of the current path and ignored the "return" part. We now know, however, that designers of high-speed circuits need to take as much care with the latter as with the former, because their PCBs won't work at all without good-quality ground and power planes.

Returning to the wave model, we can see why the path taken by the return current is as important for the guiding of the electromagnetic wave (our signal) as the send path. The physical arrangement of the send and return current paths and their insulating materials—along with the complex impedances of the source and loads—govern how much of the wave will end up being dissipated in the load, and how much of it will leak out (only to be picked up later, during EMC testing).

So all signals are electromagnetic waves, and all electrical conductors are leaky waveguides. This is just as true of a coffee machine's supply cord as it is of a digital signal on a PCB.

Another name for a leaky waveguide is an antenna. Antennas work equally effectively in the two different modes—as radiators (important for emissions) and as receivers (important for immunity). A common observation in EMC testing is that digital products that produce strong emissions at certain frequencies are quite likely to have poor immunity to external fields at those same frequencies (see Figure 1).

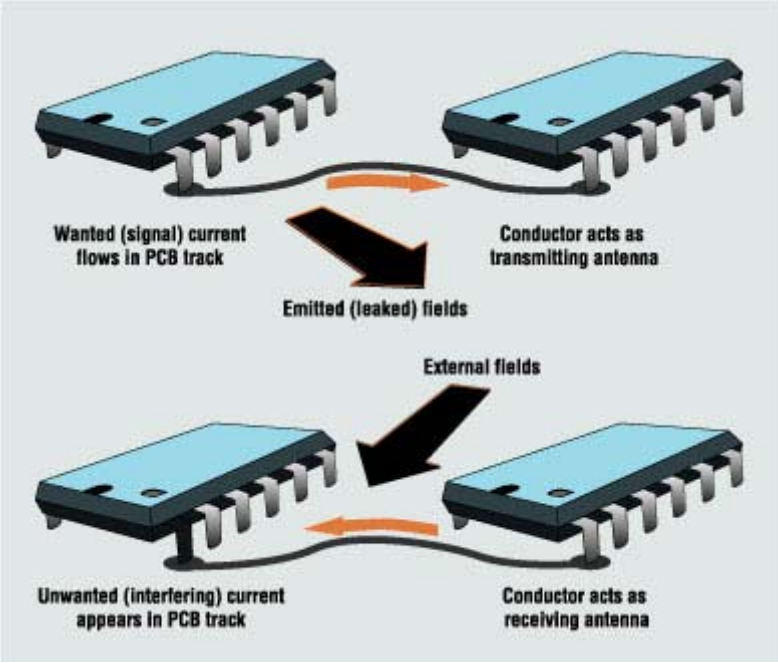

Figure 1: EMC issues and crosstalk on a PCB.

It is physically impossible to turn any signal conductor into a completely leakproof waveguide. The best that can be hoped for is to design it so that enough of the signal (i.e., the propagating wave) ends up in the intended loads to achieve adequate signal integrity, while not enough leaks off to cause EMC problems. When this is achieved, the conductor will not be a good antenna, which means it will also tend not to pick up interference. Lending itself particularly well to this sort of electromagnetic wave analysis is cross talk, which occurs when a wave propagating along one conductor leaks off and is picked up by another conductor. At low frequencies, the conductors are in each other's near field and can be analyzed simply through the use of electric and magnetic fields (i.e., as capacitive and magnetic coupling), rather than requiring full-fledged electromagnetic fields.

Signals in Both Time and Frequency Domains

Let's turn now to an example and a few figures that I hope will elucidate the relationship between signal integrity and EMC. The example cited below is a digital clock signal, but the concepts developed will hold true for any type of analog or digital signal. (Bear in mind that the situation described is a highly simplified version of what is likely to be encountered in real life. The sketches are intended only to suggest a qualitative relationship and are not printouts of actual measurements.)

This example manifests just one signal-integrity issue: a short-rise-time clock signal is sent down a PCB trace, but the trace itself is so long (at 4 in.) that it really ought to have been implemented as a transmission line instead. Because all other signal-integrity issues are so closely tied to EMC phenomena, the adoption of comprehensive EMC design techniques from the start of a project (in an effort to optimize hardware in terms of cost and time to market) will automatically address the problem of signal integrity.

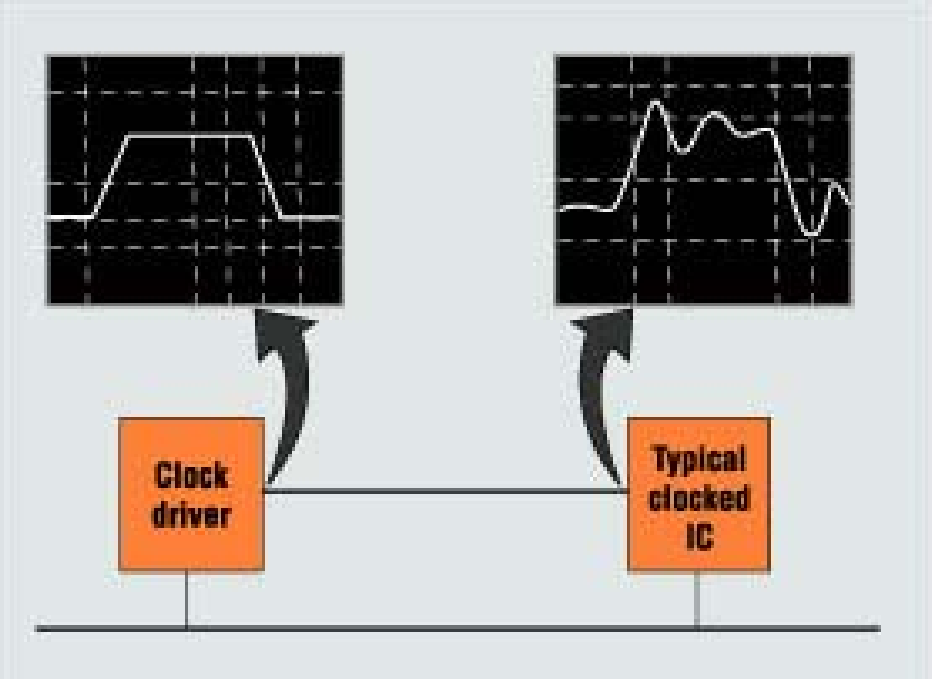

Figure 2: The signal-integrity problem as seen by an oscilloscope.

Figure 2 shows our signal-integrity example as it might appear on a high-bandwidth oscilloscope. The clock driver has a nice square output waveform, but its load IC sees a clock input waveform distorted by both overshoot and ringing. There are a number of possible reasons for this, including the following:

- The trace may not have been designed as a transmission line.
- The trace transmission-line design may be correct, but the termination may be incorrect.
- A gap in either the ground or the power plane may be disturbing the return current path of the trace.

Figure 3 shows part of the waveform of an ideal 166-MHz squarewave with 0.6-ns rise and fall times. (The sketches here are idealized—few people ever see a waveform this good.)

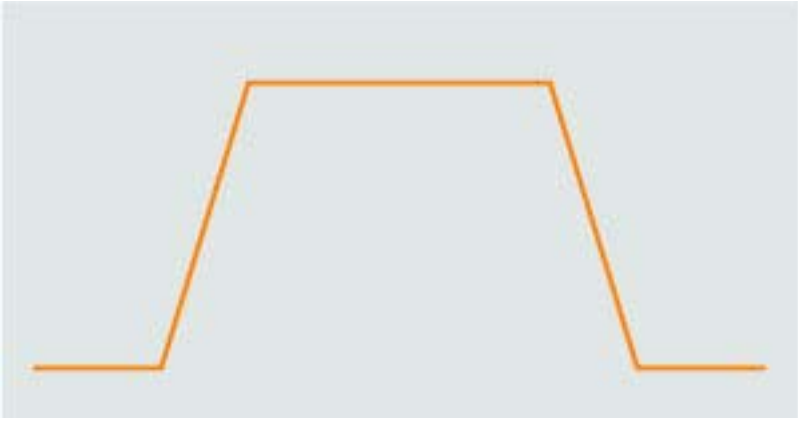

Figure 3: The waveform of an idealized 166-MHz squarewave with 0.6-ns rise and fall times.

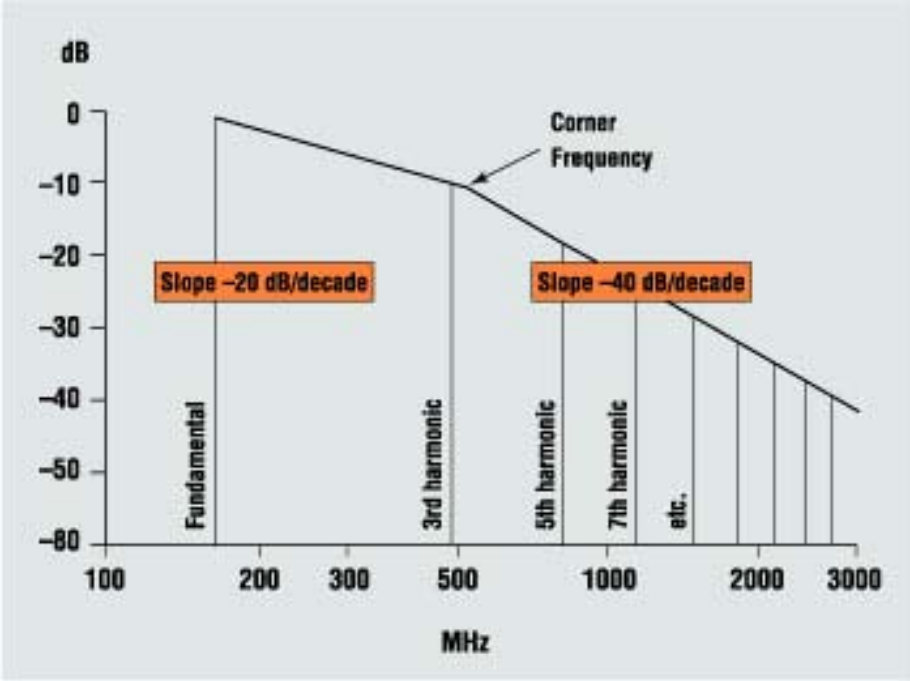

Figure 4: The spectrum of the idealized 166-MHz squarewave.

Figure 4 shows the corresponding (again, idealized) frequency spectrum for the waveform in Figure 3. A number of narrow vertical spectral lines may be seen, starting with the fundamental frequency at 166 MHz and continuing through all of its odd-numbered harmonics. (It should be noted that perfectly square waveforms display no even-numbered harmonics.) The harmonics of the clock signal extend to very high frequencies. A dotted line (which would not appear on a real spectrum analyzer) traces the envelope of the signal and its harmonics.

The declining slope of the envelope of the harmonics is –20 dB/decade up to a frequency of 530 MHz, at which point the slope increases to –40 dB/decade. The slope change from –20 to –40 dB/decade is caused by the rise and fall times of the clock's waveform, designated tr and tf. For an ideal waveform as shown in Figure 3, and with tr=tf, the "corner" frequency at which the slope change occurs can be calculated as $1/\pi tr$. Thus, when tr=tf=0.6 ns, we obtain a corner frequency of 530 MHz. Similarly, a waveform with tr = tf = 2 ns would yield a corner frequency of 159 MHz.

Textbook wisdom generally holds that the signal-integrity or EMC designer need not be concerned with the frequency content of signals above this break point, but here, as elsewhere, real life can provide some surprises. Real digital waveforms are not perfectly trapezoidal (especially when created

by saturating logic such as normal transistor-transistor logic [TTL] or complementary metal oxide semiconductor [CMOS]), so the envelope of their harmonics may not fall away as smoothly as implied in Figure 4. Then, too, data-sheet rise and fall times are maximum values, not minimum ones, and the chips used will typically have faster edges than the data sheets specify. Significant emissions at up to 1 GHz have been seen, for example, from circuits using F-series TTL, despite their rise and fall times being specified at 2 ns.

Now let's consider the antenna effect of an ideal 4-in.-long straight PCB trace on a typical FR4 glass-fiber PCB (see Figure 5). This PCB trace is assumed to be entirely isolated, with no other traces anywhere near, driven by a perfect 0-(Ω) source at one end and terminated at the other end by a perfect (infinity) (Ω) load. This antenna effect represents the leakiness of the PCB trace—that is, its imperfection as a waveguide. Because one end of the trace sees a very low impedance and the other sees an open circuit, the trace will be quarter-wave resonant. If the trace had a low (or high) impedance at both ends, it would be half-wave resonant, and Figure 5 could be corrected by doubling its horizontal-axis frequencies.

Adapting any of these sketched graphs to other situations is merely a matter of scaling. For a 1-ns rise/fall-time waveform, the corner frequency should simply be moved five times lower. For a 16.6-MHz clock, the frequency axis for the clock harmonic spectra should be multiplied by 0.1. For a 10-in.-long PCB trace, the frequency axis of the antenna effect graph will need to be multiplied by 0.4. These graphs can be very useful in the earliest design stages of a project—for instance, in deciding which nets are most critical for signal integrity and EMC.

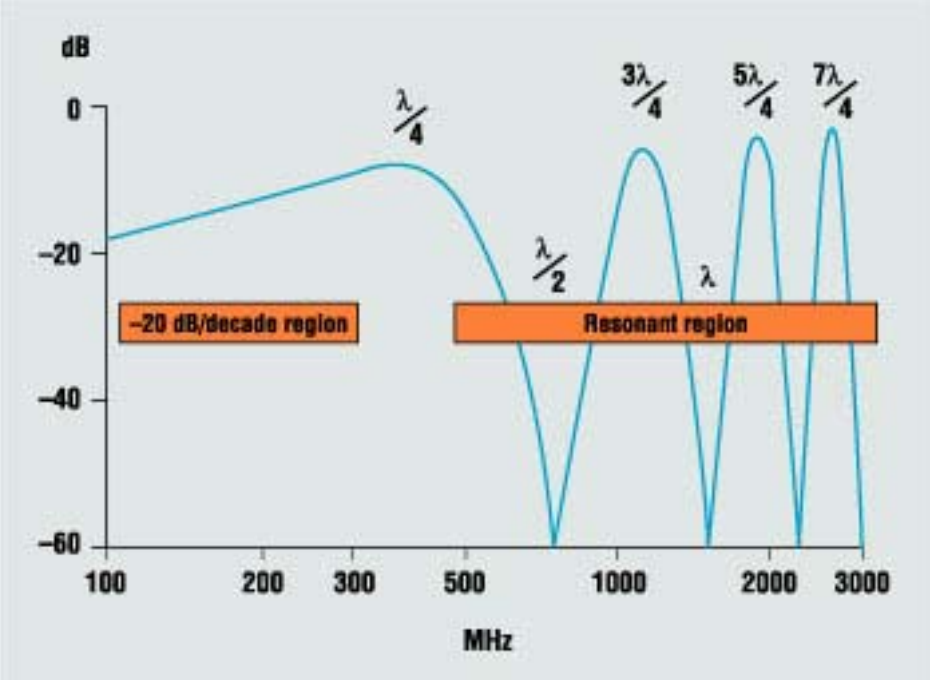

Figure 5: The "antenna effect" of an idealized 4-in.-long PCB trace.

Figure 5 shows us that the PCB trace becomes a better antenna (i.e., it leaks more) as frequency increases, smoothly reaching its first peak when its electrical length equals one-quarter of a wavelength. Because the trace is on FR4, which has a relative dielectric constant of around 4.0 at high frequencies, the velocity of propagation is around one-half what it would be in free space, meaning that the electrical length of the trace is almost twice its actual length. When the voltage in the trace experiences voltage maximum at a resonant point like this, the current in the trace experiences a minimum.

At frequencies higher than the first resonance, the antenna effect of the trace varies regularly between deep troughs and increasingly higher peaks. At frequencies for which the electrical length of the trace equals an even-numbered multiple of quarter wavelengths (i.e., half or full wavelengths), there are deep troughs in the "antenna effect"—or voltage minima—that correspond to current maxima. At frequencies for which the electrical length equals an odd-numbered multiple of quarter wavelengths, there are new peaks—or voltage maxima—that correspond to current minima. The corresponding graph of antenna effect for a trace implemented as a properly terminated transmission line would be a

fairly straight line never exceeding about –40 dB and having no resonant peaks or troughs, no matter how long it was.

Now let's see what happens when we measure the spectrum at the load end of the ideal 4-in. trace (with its antenna effects) when it is sourced from the ideal 166-MHz waveform. Figure 6 shows that the load end is lacking some spectral content. Notice that the peaks and troughs of Figure 5 correspond to those in the harmonic content of the signal voltage at the load (see Figure 6).

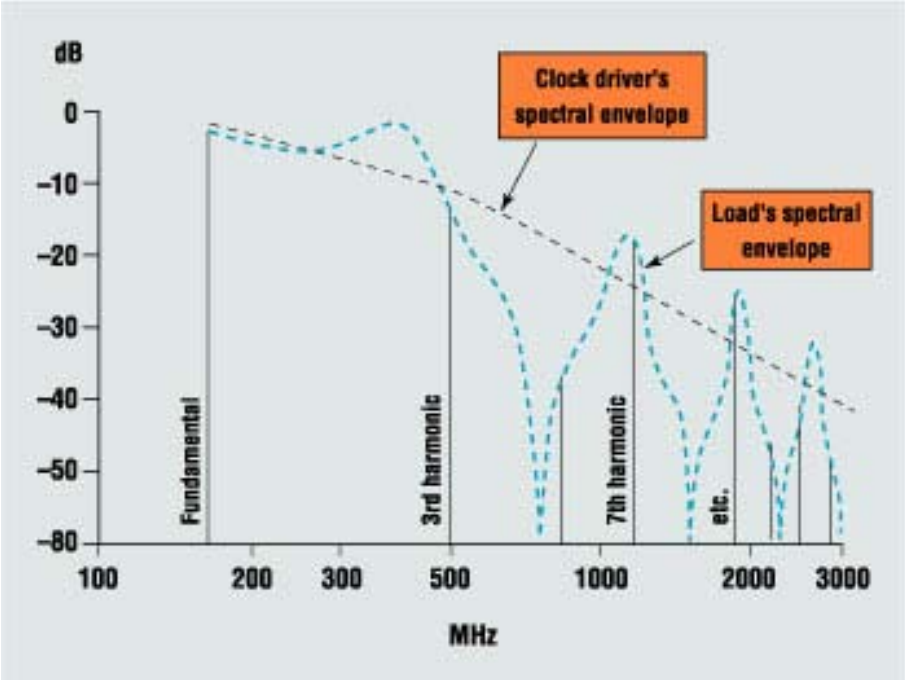

Figure 6: The spectrum of the distorted waveform at the load.

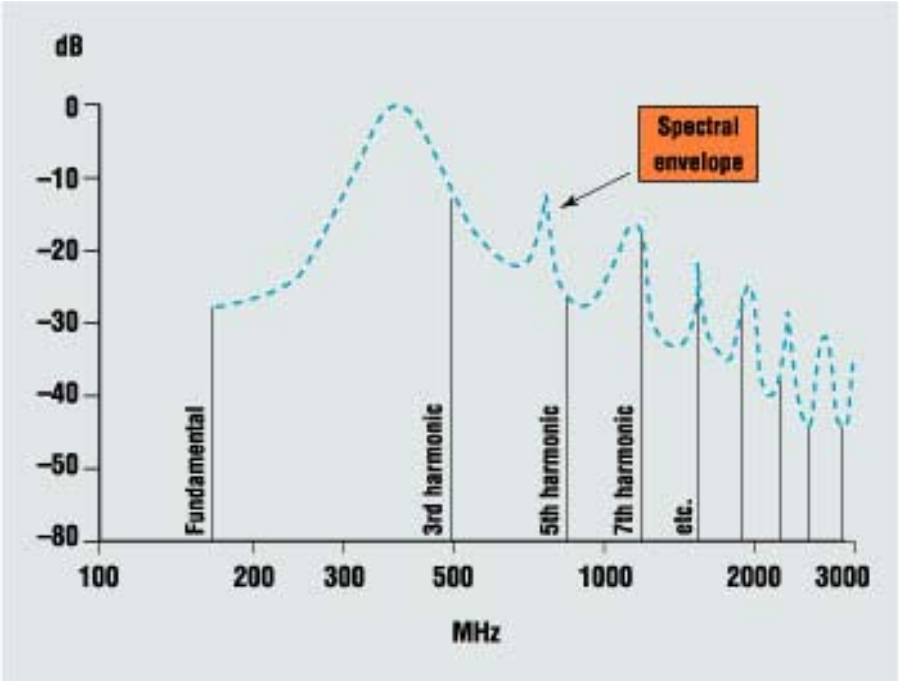

Figure 7: The spectrum of the radiated emissions from the 4-in. trace.

Figure 7 shows the spectrum of the radiated emissions from the ideal 4-in. trace, revealing peaks at the frequencies where Figures 5 and 6 display either peaks or troughs. At the peaks in Figures 5 and

6, the trace is emitting (i.e., leaking) wholly electric fields, whereas at the troughs the trace is emitting wholly magnetic fields. Notice that the third and fifth harmonics of the clock signal do not coincide with their nearby peaks in the trace's antenna effect. If the trace were just a little shorter, the antenna peaks would be a little higher in frequency and could tune in these harmonics, which might then have emissions about 10 dB worse. The seventh harmonic is already almost exactly on a peak, so a slightly shorter trace that increased the emissions of the third and fifth harmonics would probably reduce the emission levels of the seventh.

The foregoing demonstrates how a simple modification to a PCB can strongly affect its EMC and signal integrity, and, by extension, how it might easily cause a product to become noncompliant or unreliable or both. PCBs that benefit from properly designed-in EMC are much more forgiving of small design changes, so as well as being more competitive at its launch, a product that uses such PCBs will carry a lower risk of unforeseen dips in profitability over its lifetime.

EMC emissions measurements are made with an electric-field antenna in the far field, where the electromagnetic waves from the product are fully developed. No matter whether an emission starts out as an electric field or as a magnetic field, it will always become electromagnetic in the far field, where a proper EMC emissions test will detect it. To complete the picture, Figure 8 graphs all the waveforms for the example circuit: the clock source, the load, and the radiated emissions.

The signal at the load shows a slowed rate of rise and fall as well as significant overshoots and undershoots. The slow edges worsen the skew, and the over- and undershoots can cause false triggering if they cross logic thresholds. Even where the ringing does not cross such thresholds, however, it reduces noise margins, making the circuit more vulnerable to both internal noise and external interference.

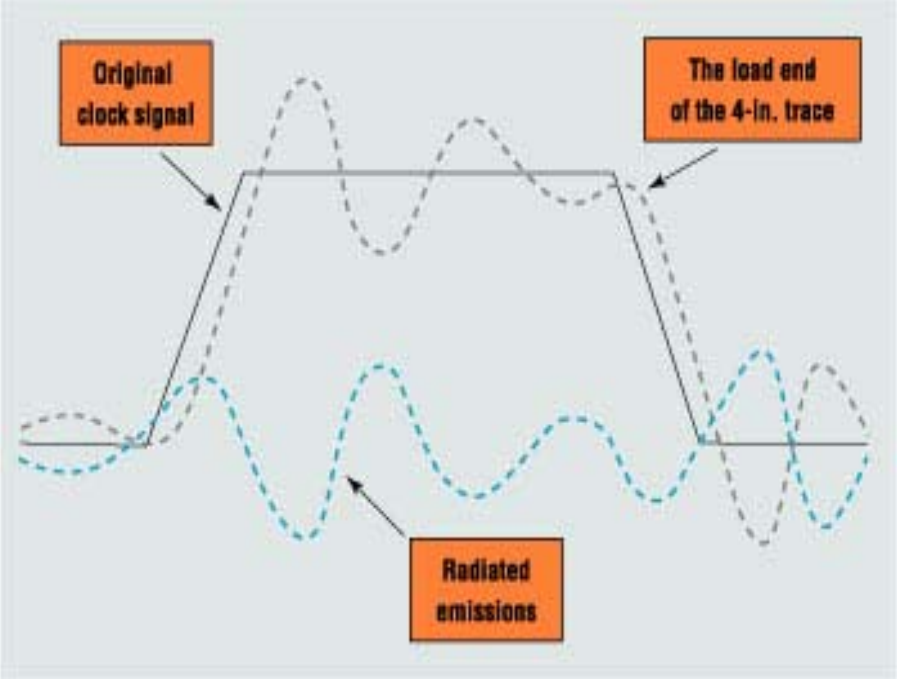

Figure 8: The final waveforms.

Most people will be unfamiliar with the waveform of the radiated emissions shown in Figure 8. If a spectrum analyzer used in a proper EMC emissions test was to be replaced by an oscilloscope, this waveform would still not be visible because the antenna used would pick up too many other signals from the product, in addition to ambient interference. A close-field magnetic-loop or electric-field probe connected to an oscilloscope, though, might be able to describe the different contributions to this waveform fairly well, as such probes respond only to nearby emissions.

When an insulated close-field probe is held directly against a trace, it will pick up the currents or voltages in the trace itself, which can also provide some useful information. Close-field probes can be very powerful tools when used during the development of hardware, and can pinpoint EMC and signal-integrity problems even on a first-prototype PCB.

Using Oscilloscope Measurements to Gauge EMC Performance

When we measured a signal with a voltage probe and an oscilloscope and discovered that the waveform became degraded as it traveled from source to load, it was clear that we might have some

signal-integrity issues. Figure 8 demonstrates that the same measurement can also reveal EMC and cross-talk problems. The main ringing frequencies on the scope picture are often the worst frequencies for EMC emissions, as well as probably the worst for immunity.

High-speed oscilloscope measurements can, in contrast, indicate that signal integrity is very good and that EMC compliance is going to be a breeze, where the results show that the source and load waveforms

- Are identical for each node or net.
- Have rise and fall times at least as fast as the data-sheet specifications.
- Have very small amounts of overshoot and ringing.

It is not terribly difficult, therefore, to predict the radiated emissions and immunity performance of a digital circuit merely by using an oscilloscope (though this method cannot result in quantitative accuracy or account for the effects of filtering, for example at I/O ports). Still, some caveats are in order here. When used for high-speed or EMC measurements, an oscilloscope must have sufficient bandwidth and must employ the proper high-bandwidth probes. Correct high-speed probing techniques, which may be found in the application notes provided free by oscilloscope manufacturers, are also essential. Poor technique—as exemplified by long-probe ground leads or inappropriate test-bench setups—can produce overshoots, ringing, and noise. And most important: Never disconnect an oscilloscope's protective ground lead.

Conclusion

Because, as we have seen, EMC and signal integrity are really just two different aspects of the same electronic phenomenon, using good EMC design and PCB layout practices from the start of a new project can help

- Achieve signal integrity.
- Reduce the number of prototype iterations needed and improve time to market.
- Cut unit manufacturing costs.
- Lower the risk that modifications made during the product's lifetime may inadvertently cause noncompliance or unreliability.

The graphs presented in this article may be easily adapted to a wide variety of signals and PCB trace lengths, even in the earliest design stages.

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