



Another EMC resource
from EMC Standards

Doing SI, PI and EMC right first time

Helping you solve your EMC problems



**Simulators for SI, PI, EMC can
minimise / eliminate design iterations,
and justifying their high cost is easy**



Keith Armstrong
Independent EMC design consultant since 1990
www.cherryclough.com
keith.armstrong@cherryclough.com



Doing SI, PI, EMC *right first time*

- Computer motherboard manufacturers have been achieving right first time design for SI, PI and EMC, for over 20 years...
 - using computer-aided engineering tools that originally cost \$1million per seat
- They had to, because their product's sales life was only 90 days...
 - so they had no time to fail any tests and iterate any PCBs, even once



Doing SI, PI, EMC *right first time* (2)

- The CAE tools they use are now much better...
 - and much less expensive (approx. \$250,000)...
 - and easy to justify financially because they can pay back on the first project...
 - or in the first year
- Let's take a quick look at how they help us get to market as quick as possible...



Doing SI, PI, EMC *right first time* (3)

- Circuit designer uses SPICE or IBIS simulators...
 - to prove the initial schematic meets the SI and PI targets and functions as specified...
 - the main problem can be getting accurate SPICE or IBIS models of new ICs in time



Doing SI, PI, EMC *right first time* (4)

- Circuit designer netlists the completed schematic to the PCB designer...
 - and also specifies the electrical issues which depend on aspects of PCB design, e.g...
 - critical component placements, noise margins, crosstalk limits, skew limits, max propagation times, characteristic impedances, max inductances, etc...
 - all with their associated tolerances



Doing SI, PI, EMC *right first time* (5)

- PCB designer does the initial board placement and layout...
 - then chooses simulation models for all components (active or passive)...
 - not already chosen by the circuit designer...
 - and for any cables/connectors...
 - then uses Field Solvers to create models of certain structures (e.g. connectors, large/tall components) for which no models are available



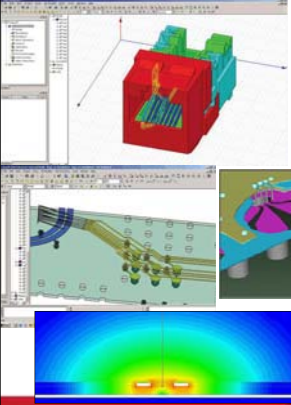
Member



Member



Q3D Extractor® – 2D & 3D Solver



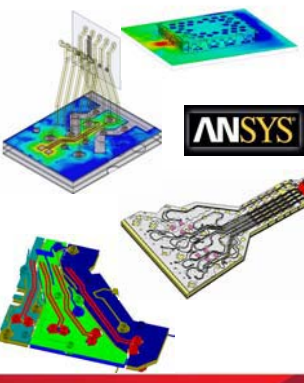
ANSYS

- Quasi-static EM simulator for arbitrary 2D & 3D “electrically small” structures
- Intuitive, easy to use Windows GUI extracts:
 - per-unit-length RLGC (frequency dependant)
 - transmission-line parameters
 - characteristic impedance (Z_0) matrices
 - propagation speed, delay, effective permittivity
 - differential and common-mode parameters
 - near- and far-end crosstalk coefficients

Creation of equivalent circuit SPICE models
 Options: Multicore and Optimisation
 Dynamic link with Designer SI

EMC LIVE
 RESIN BOOTCAMP

Ansoft HFSS™ – 3D Solver



ANSYS

- Fullwave electromagnetic simulator for arbitrary 3D “electrically large” structures
- Intuitive and easy to use Windows GUI
- SPICE export
- Full-Wave Spice – Broadband Mode
- Lumped RLC – Low Frequency Model
- Partial Fraction – Matlab
- HSPICE, PSPICE, Cadence Spectre
- S-Parameter export (Z, coupling, crosstalk, reflection coeff...)
- Advanced Material Handling (lossy, frequency dependent dielectrics, ...)
- Options: Multicore, Optimisation & Distributed Computing
- Dynamic link with Designer SI
- Plot radiation fields (EMC)

EMC LIVE
 RESIN BOOTCAMP

Doing SI, PI, EMC *right first time* (6)

- PCB designer then uses a Field Solver to extract critical PCB characteristics (R, L, C; prop. delay; ground bounce; Z_0 ; etc..) from the 1st draft board layout...
 - and sends them back to the circuit designer for inclusion in the circuit simulation
- These are the strays / parasitics that make up the (so-called) “hidden schematic”...
 - and cause SI (crosstalk, signal distortion, poor noise margins, poor S/N ratios, etc.) PI and EMC problems

EMC LIVE
 RESIN BOOTCAMP

Doing SI, PI, EMC *right first time* (7)

- **Now here’s the clever bit...**
 - the circuit designer re-simulates the schematic using SPICE or IBIS...
 - with the critical “hidden schematic” board layout parameters automatically included...
 - no human can do this (much too complex)...
 - and modifies the design as necessary to meet all the spec’s

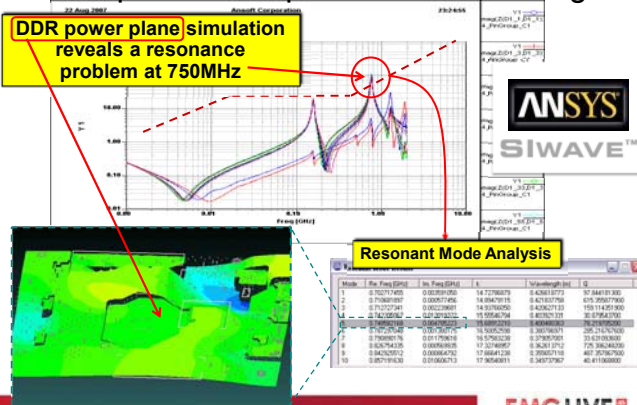
EMC LIVE
 RESIN BOOTCAMP

Doing SI, PI, EMC *right first time* (8)

- Circuit designer then netlists the 2nd draft design to the PCB designer...
 - along with any requests for changes in component placement, routing, etc.
- PCB designer and circuit designer repeat the above steps...
 - iterating the *virtual* design until both are happy with the results

EMC LIVE
 RESIN BOOTCAMP

Example: one step in a virtual PI design



ANSYS SIWAVE™

DDR power plane simulation reveals a resonance problem at 750MHz

Resonant Mode Analysis

Mode	Re. Freq (GHz)	Im. Freq (GHz)	Q	Wavelength (mm)	Q
1	0.75000000	0.00000000	14.278675	0.40618772	30.04617300
2	0.75000000	0.00000000	14.85670175	0.411637768	315.35267700
3	0.75000000	0.00000000	14.91700000	0.412631123	159.14426700
4	0.75000000	0.00000000	15.00000000	0.415000000	30.00000000
5	0.75000000	0.00000000	15.50000000	0.420000000	30.00000000
6	0.75000000	0.00000000	16.00000000	0.425000000	30.00000000
7	0.75000000	0.00000000	16.50000000	0.430000000	30.00000000
8	0.75000000	0.00000000	17.00000000	0.435000000	30.00000000
9	0.75000000	0.00000000	17.50000000	0.440000000	30.00000000
10	0.75000000	0.00000000	18.00000000	0.445000000	30.00000000

EMC LIVE
 RESIN BOOTCAMP

Doing SI, PI, EMC *right first time* (9)

- In 2007, that PI simulation took 7 minutes on a good-quality desktop PC...
 - it took 4 iterations to ‘tame’ the DDR power plane problems by adding decouplers, with no impedances > 50% of the PI spec...
 - 40 minutes overall, but modern PCs are much more powerful, and cost less
- Notice other power plane resonances...
 - that still remain to be fixed, and then there are the other layers to simulate and fix



Doing SI, PI, EMC *right first time* (10)

- Finally, the PCB designer runs a complete extraction of all board characteristics...
 - not just what had been assumed would be critical...
 - and the Circuit designer runs a SPICE/IBIS simulation with the full ‘hidden schematic’...
 - as a final check that nothing has been overlooked
- These simulations need powerful computers if we want to have them done in a day or so



Doing SI, PI, EMC *right first time* (11)

- Then the Circuit designer runs Monte-Carlo (or similar) analysis...
 - to see whether real-life tolerances & variations (e.g. initial tolerances, aging, tempco’s, etc.) will still allow all the specifications to be met...
 - and ensure that the board manufacturing tolerances required are within the chosen manufacturer’s capabilities...
 - modifications may be needed to both the *virtual* schematic, BOM and *virtual* PCB layout



Doing SI, PI, EMC *right first time* (12)

- For a PC with typical shielding / filtering...
 - a motherboard designed in this way can proceed directly to manufacture...
 - knowing that all technical spec’s for SI, PI and EMC will be met with a good yield in production
- **No physical prototyping!**
 - and no pre-compliance testing or design re-spins...
 - the first motherboard actually assembled can be immediately sold to a customer



Doing SI, PI, EMC *right first time* (13)

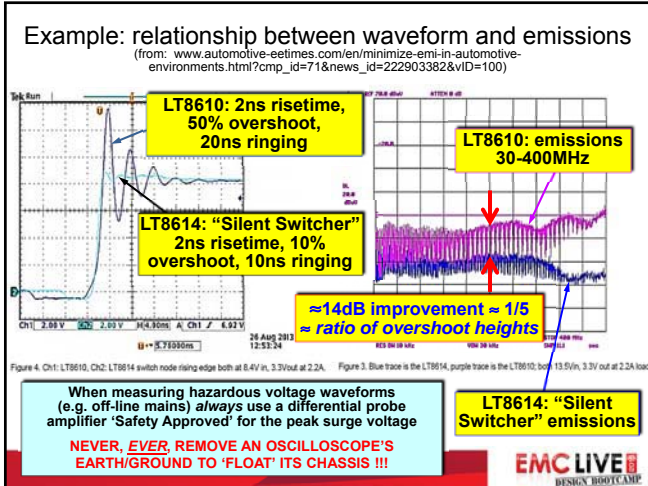
- **This virtual design process is well-proven to be 100% accurate for SI and PI...**
 - but there are (as yet) no simulation tools for *precisely* determining what will be the EMC emissions and immunity...
 - for the final PCB(s) assembled in the final enclosure(s) and connected to cables...
 - however, the tools are getting much better and (with a bit of EMC competence) can be used to specify the filters, shielding, etc., required



Doing SI, PI, EMC *right first time* (14)

- There is an (almost!) perfect relationship between SI, PI and EMC...
 - the ‘cleaner’ and less distorted the waveforms, the lower the emissions (and *vice-versa*)
- For a modern PC motherboard, good EMC for digital and DC/DC converter circuits can generally be achieved...
 - by setting 5 to 10 times tougher limits for SI and PI than are needed to meet the functional spec’s





Doing SI, PI, EMC *right first time* (15)

- Digital circuits' emissions and immunity are generally closely related...
 - i.e. frequencies at which emissions are higher, will be more susceptible...
 - e.g. passing CISPR 22 Class A emissions typically means passing CISPR 24 immunity (±6dB or so)...
 - where radiated/conducted immunity test levels are higher than 3V (whether rms or per meter)...
 - emissions (hence SI and PI spec's) should be correspondingly lower than CISPR 22 Class A



Doing SI, PI, EMC *right first time* (16)

- Low-frequency analogue circuits don't have appreciable RF emissions, when operating linearly...
 - but beware of RF emissions caused by overdrive, clipping, instability...
- but all are susceptible to >1GHz noise...
- so simulating the RF resonances of conductors and components (i.e. their "accidental antenna" behaviour) is a powerful technique for EMC design



Doing SI, PI, EMC *right first time* (17)

- Achieving good EMC by achieving much better SI and PI specifications, gives the *lowest overall cost of manufacture*...
 - because it costs much less to achieve EMC by spending more on BOMs and boards...
 - than adding filtering/shielding after failing tests...
 - and also saves project cost/time, getting new products to market more quickly...
 - by quickly/easily meeting functional spec's and so reducing (eliminating?) the number of design respins

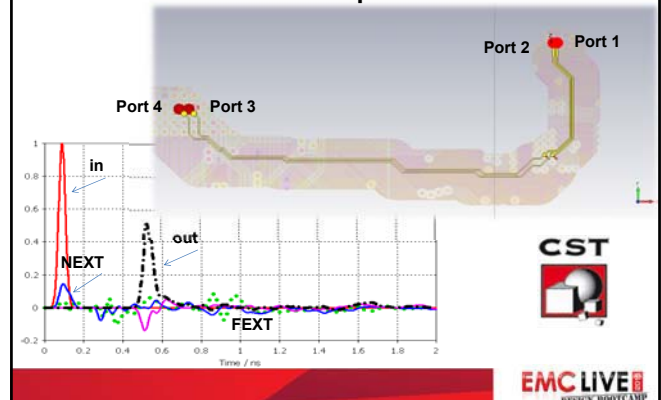


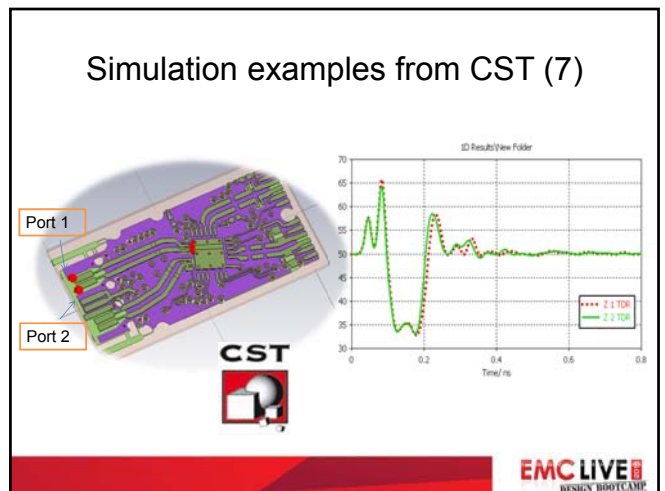
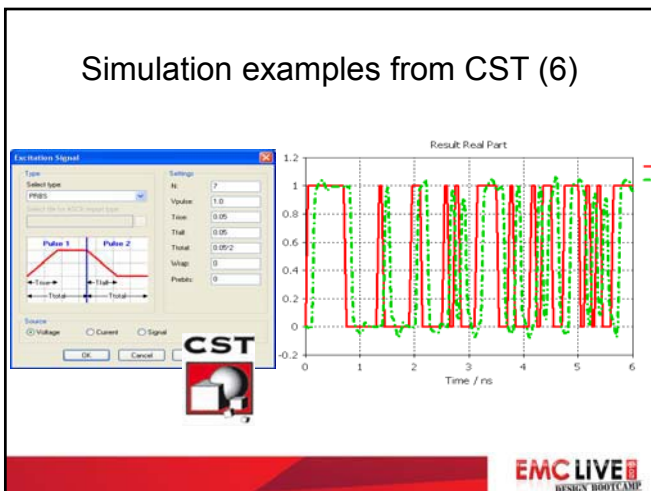
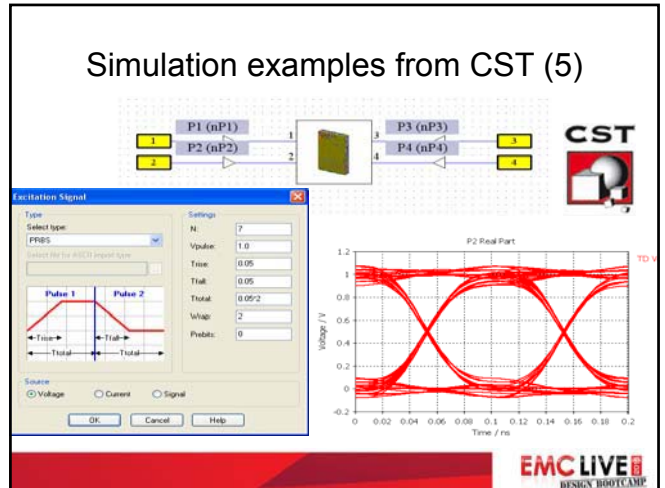
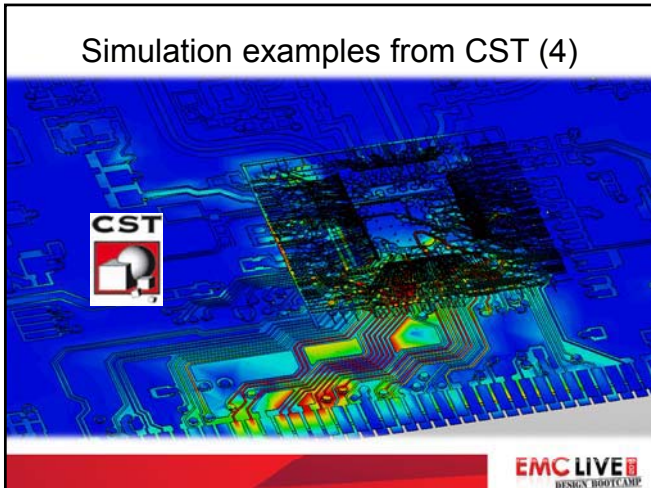
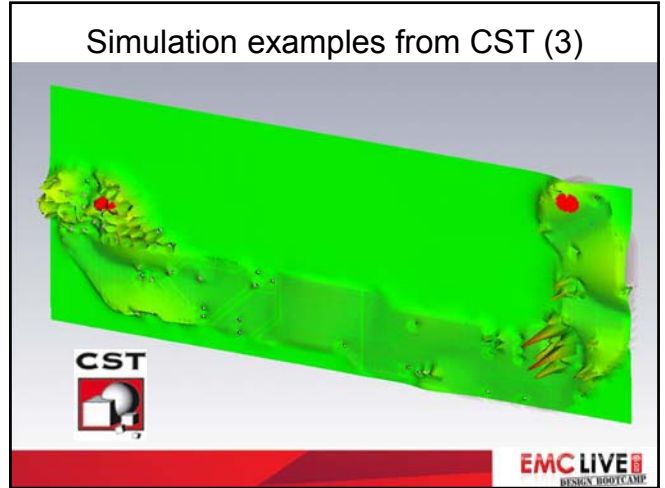
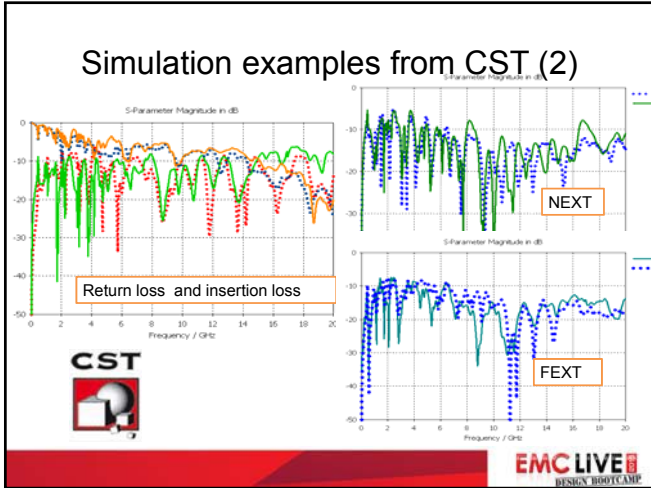
Doing SI, PI, EMC *right first time* (18)

- Of course long power cables will need filtering and surge suppression...
 - and signal cables will need filtering / shielding / ESD / surge suppression, and some/all PCB areas may need board-level-shielding...
- but it is easy to make provision for them, (using proven good EMC design practices)...
 - because ensuring that every board's SI and PI is 5 to 10 times better than needed for functionality, means few/no EMC surprises...
 - e.g. from unexpected RF resonances



Simulation examples from CST





Justifying the purchase of the required simulators

- Most companies are run for purely financial reasons these days...
 - by non-engineers, usually financial people...
 - who don't understand what it is that we engineers actually do...
 - or how we do it...
 - even if they were once engineers...
 - they will probably have been overwhelmed by financial issues and not be up to date with design



Justifying the purchase of the required simulators (2)

- To do our engineering for the best financial performance of our employers...
 - we need to provide them with the information they need to manage us effectively
- But they only understand 'finance-speak'...
 - which we engineers must learn in order to communicate effectively with them...
 - *because there is no way they are ever going to understand our language !*



Justifying the purchase of the required simulators (3)

- We only need to use gambling language...
 - A) What is the value of the prize?
 - the Return On Investment: ROI
 - B) How much is the stake?
 - the amount invested
 - C) When is the break-even point?
 - when investment + interest is paid back
 - D) What is the likelihood of success?

We must use this order !!!



Justifying the purchase of the required simulators (4)

- We must limit our communications with managers to issues of...
 - Money (always stating the prize value first!)
 - Time
 - Probability
 - with any/all engineering issues summarised *in plain normal everyday language...*
 - using no technical terms, mathematics, acronyms, jargon, standards numbers (e.g. CISPR 22) **at all !**



Justifying the purchase of the required simulators (5)

- To be able to make such a 'business case' requires assessing *all relevant issues* for the *entire* organisation, *and* costing them...
 - ± 30% (or worse) accuracy usually good enough, (it is usually impossible to do any better!)
 - yes, this involves doing more work, *and* moving outside our comfort zone, *and* making imprecise estimates...
 - and yes, it is a cruel, hard world – but huge rewards await those who take on this challenge!



Justifying the purchase of the required simulators (6)

- Our managers *will* take our ideas and present them as being their own...
 - to make themselves look good in front of their peer group (other managers) and bosses...
 - but *we must not mind this...*
 - we engineers will be getting what we need to help make our organisation more successful...
 - and our managers will always remember who it was that made them look good!



Justifying the purchase of the required simulators (7)

- What we are really talking about in this webinar is reducing 'financial risk'...
 - i.e. the uncertainty in the time it will take to (successfully!) bring a new product to market...
 - bearing in mind the large financial investment that has gone into its design, development, preparations for manufacture, marketing, etc...
- very much more than just the cost of our salaries



Justifying the purchase of the required simulators (8)

- Purchasing a simulator for \$250,000...
 - being trained on it, and using it fully...
 - could easily save a months' time to market (with, say, a 50/50 probability)...
 - which the Sales/Marketing boss might say was worth \$1 million
- There is *always* money available for investment in a 'no-brainer' like this!
 - if we make our proposal in the right way



Justifying the purchase of the required simulators (9)

- Most financial managers/bosses would be *totally appalled* by the financial risks their organisations are unwittingly exposed to...
 - by engineering decisions that we engineers take on our own...
 - without discussing with them first...
 - *because they can't speak our language!*
 - *and we don't speak theirs!*



Justifying the purchase of the required simulators (10)

- I sincerely believe that the lack of effective communication between engineers and their managers...
 - is what is holding most design/manufacturing companies back
- I see a lot of 'low hanging fruit' in most organisations...
 - where effective communication and understanding would pay back handsomely, and often very quickly



Justifying the purchase of the required simulators (11)

- The intelligent use of costly simulators will soon make all the difference...
 - between companies bringing ever-more-complex electronics to market on time...
 - without most being returned under warranty, or alienating their market with high costs, poor performance or too-many bug-fixes...
 - and the companies sliding towards oblivion...
 - because their engineers cannot effectively communicate what they need, to their managers



Thanks for attending!

Don't miss our 3 day event in April!
April 28-30, 2015
www.emclive2015.com



Member



Member

