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Designing I/Os so they will not suffer from 'ground
loop' currents in cable screens (shields)

Helping you solve your EMC problems

Designing I/Os so they will not suffer from ‘ground loop’ currents in cable screens (shields)

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In the previous Issue of the EMC Journal [1] I wrote about the various ways of terminating cable screens (shields). I made the point that bonding a cable’s screen at *both* ends was generally recommended for new designs, and 360° bonding – sometimes called circumferential or peripheral bonding – at *both* ends will generally achieve the best EMC possible from the type of cable used, at the lowest cost.

Unfortunately, legacy design and construction considerations can make it undesirable to directly bond the screen at both ends, so the article went into the various alternatives available, describing their pros and cons.

I happened to mention once or twice in [1] that it would have been so much better if all electronic engineers had taken the trouble to design their products and equipment correctly. Their customers would then have found it much easier to interconnect equipment in systems and installations of any size, while using direct screen bonds at both ends to maximise EMC whilst keeping costs low.

When I mention ‘EMC’ I am referring to the whole business of controlling electromagnetic interactions both inside and outside products, to help ensure that products will be quick and easy to design and market; will function excellently in real life (keeping customers happy) and will earn good profits for their manufacturers [2].

All electrical power and signals, whether their energy is communicated by conductors or waves in the air, are electromagnetic, so “EMC engineering” has a huge scope, and a huge relevance to every kind of electrical and electronic design.

But when I am referring to the *very tiny* subset of EMC that is concerned with compliance with standards, directives, import regulations, etc., I use appropriate terminology to indicate the restricted scope.

Traditionally, many electronic engineers failed to design their input and output circuits (I/Os) for the earth (ground) potential equalising currents that inevitably flow in cable screens when they are connected at both ends to different items of equipment that receive their power from different parts of a building, vehicle or site.

These screen currents have been demonised for the last 50 years at least, by some electronic engineers – and (apparently) by all electrical contractors and installers – as “earth loops”, “ground loops”, “hum loops” and other less well-known jargon terms.

So how do we design input and output circuits so that they are not significantly affected by screen currents? It’s easy:

Do not allow ‘ground loop’ currents to cause significant ‘ground noise’ voltages to arise in a circuit’s 0V reference.

The earth/ground potential difference that appears on a cable connected to a separate item of equipment appears as a common-mode (CM) noise voltage. This is easily dealt with by using a circuit that provides adequate CM rejection (CMR).

The best input or output circuits for CMR use differential (balanced) signalling techniques, typically using twisted-pair conductors with an overall screen. In such cables, capacitive coupling between the screen and the internal conductors is never perfectly balanced, so a differential-mode (DM) noise appears, especially when input impedances are lower.

If this DM noise lies within the bandwidth of the wanted signal it cannot be removed by filtering or phase-sensitive detection. In this situation it is important to use cables that have adequate capacitive balance for the signal-to-noise ratio (SNR) required given the earth/ground potential differences that might occur in real-life.

When a screened (shielded) cable is used with its screen directly bonded at both ends, the earth/ground potential between the items of equipment drives an equalising current in the screen. The amplitude of this current is set by the potential difference divided by the impedance of the screen and its bonds.

The screen current couples with the internal conductors like a very well-matched 1:1 transformer, and so *reduces* the CM voltage seen by the input or output [3]. So, for this contributor to the noise, all that is required is for the I/O to have sufficient CMR.

I am assuming here that the cable screen is of a type that provides a useful amount of radio frequency (RF) screening (shielding), and so completely surrounds the inner conductors. If a screen was sufficiently 'unbalanced' with respect to its inner conductors, it is possible that a current in it could induce some differential-mode (DM) noise between two or more conductors, but such a construction would be ineffective for RF and so bonding it at both ends would provide few/no RF benefits.

Since bonding at both ends to achieve EMC benefits over all frequencies is the purpose of this discussion, such cable types are not considered here.

Since screen currents act to reduce the CM voltage, why have the 'ground loops' caused by bonding screens at both ends become so demonised? As I said earlier, it is all because of bad electronic design.

I say this not because of some academic theory or benchtop experiment, but because over 28 years ago *I was that bad designer*.

The very high-performance circuits (when measured on the test bench, according to the specification I had been given) I designed were very difficult indeed to use in systems and installations. But since everyone else in my limited experience at that time designed circuits with the same problem, it took me a while to realise there had to be a better way, and what it was.

It turns out that this better way helps achieve low-cost regulatory EMC compliance; improves functional performance, and saves a great deal of time and effort in system integration and installation (see [2] for more on this).

The bad design practices that my colleagues and I were guilty of all those years ago, (and some designers still use) were:

- a) using traces on our printed circuit boards for our 0V reference, and
- b) connecting the screens of our input and output cables to those traces.

We did this because that was how we got the best functional performance on our test benches, and because "everyone knew" that this was correct design.

The design 'trick' we were missing, was to reduce the amount of 'ground noise' voltage arising in our circuit 0V reference structures, due to the low-frequency screen currents that inevitably flowed through them.

As already mentioned above: digital and analogue I/Os can easily be designed to have adequate CMR, using transformers and other circuit techniques and differential ('balanced') signalling techniques that use two conductors driven in antiphase.

Single-ended communications should never be used between items of equipment that can have significant earth/ground potential differences, except for:

- i. RF, where inputs and outputs are automatically tuned to pass the wanted frequencies and reject 'earth/ground loop' noise
- ii. Digital signals where the 'noise margin' is adequate to cope with the noise

- iii. Fixed-frequency instrumentation using phase-sensitive detection, where the frequency of operation can be set to avoid the major noise frequencies

Nevertheless, some designers have used single-ended communications with weak signals that cannot be filtered to remove 'ground loop' noise, such as video over 75Ω coaxial cable. The resulting 'hum bar' problems with video spawned a whole industry dedicated to mitigating its problems [4]. Even with such thoughtless (but low BOM cost! [2]) system design, we can still improve the noise performance of our products by taking care to ensure that the cable screen currents do not interfere with our circuits.

Traditionally, the spectrum of the earth/ground potential was dominated by the mains power distribution (50, 60 or 400Hz) and its harmonics extending to 2kHz, and possibly even to 10kHz. In telco (and now 'blade server') rooms powered from 48Vdc, the CM voltage can include appreciable levels at 0Hz.

The increasing use of variable-speed AC motor drives is now adding noise at the motor drive frequencies (say 0.1 to 120Hz) and their harmonics (say up to 12kHz) plus switching noise from their pulse-width-modulation (PWM), generally between 1 and 250kHz, plus *its* harmonics.

Because of the non-linearity of mains rectifiers, all these frequencies intermodulate madly to produce a veritable forest of spikes in the noise spectrum, from almost DC to radio frequencies.

This type of noise is bound to increase in all installations, as variable-speed motor drives are employed in all domestic appliances, HVAC and industrial machines, to help reduce electricity consumption, reduce CO₂ emissions and save the planet from overheating.

Cable-screen bonding for EMC ensures that – above some frequency – the external interfering currents are forced by the skin effect to flow on the outside surface of the screen, while the stray CM emissions from the twisted-pair (or the return current in a coax), flows – by the same mechanism – on the inside surface of the screen.

Section 2.6.2 and Figure 2P in [5], reproduced below as Figure 1, describe how this keeps the noisy external currents out of the sensitive circuits.

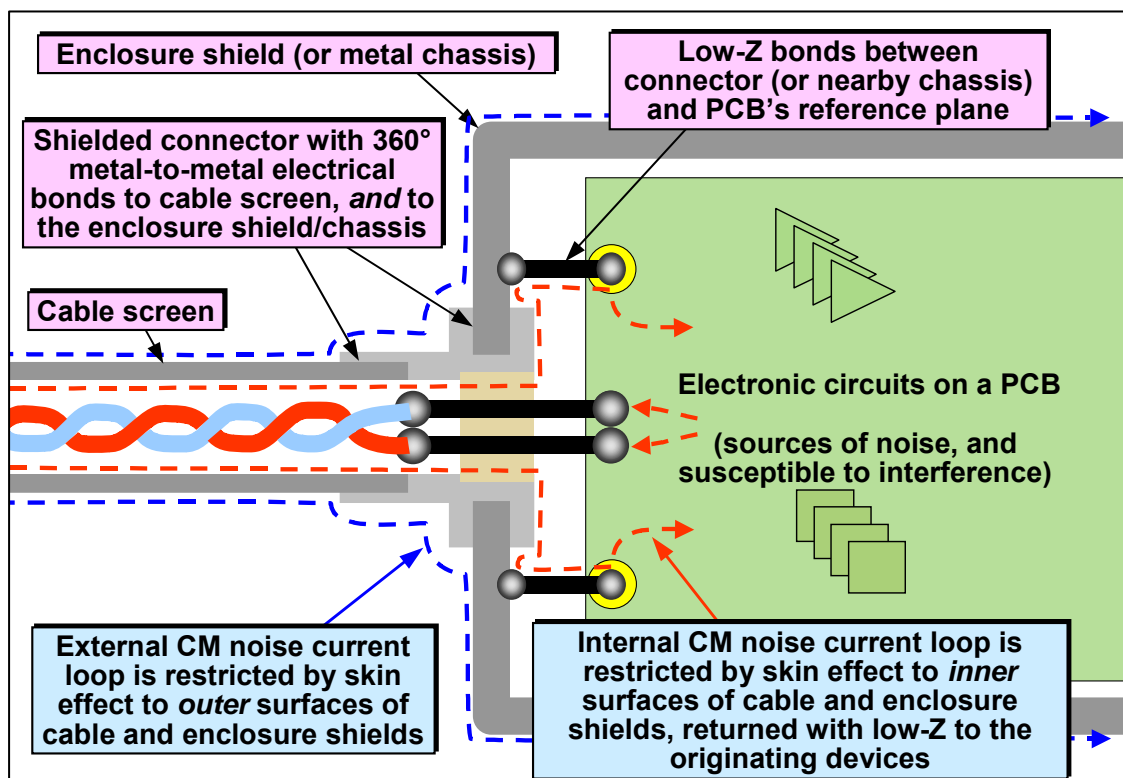


Figure 1 Cable screen bonding for good EMC at RF

Figure 2 shows a graph of skin depth versus frequency for three common metals, and [6] will also be useful.

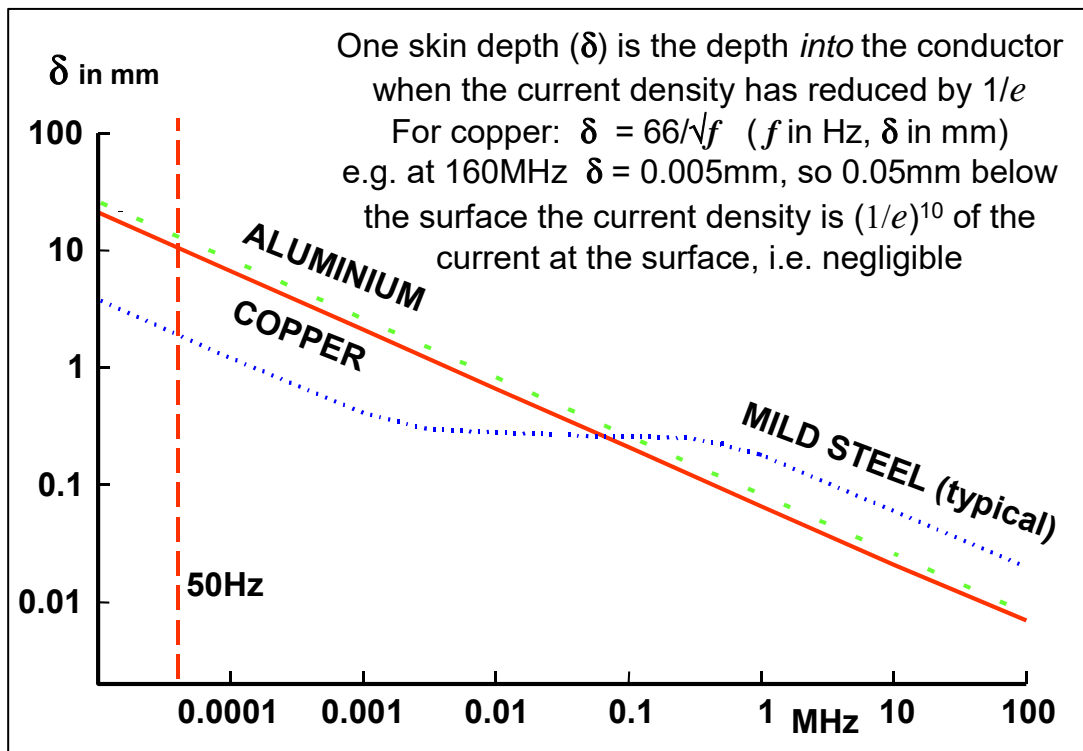


Figure 2 Skin depth versus frequency

When the thickness of the screen material for skin depth is insufficient to maintain an adequate separation of surface currents – which might be because the metal is very thin (e.g. metallised foil), or because the frequency is low – the screen current flows throughout the thickness of the shield, and we cannot them from flowing *inside* our product.

At such (low) frequencies, the prevention of excessive ‘ground loop’ noise depends entirely on providing very low impedances for the loop currents to flow in, to minimise the ‘ground noise’ voltages that inevitably appear as they flow in our circuit’s 0V reference structure.

To be able to use simple examples, let’s consider just low frequencies, say up to 1kHz, and assume that all that matters is resistance. (At higher frequencies inductance becomes the dominant contributor to the impedance, but the same analysis applies and the techniques described below become even more effective.)

It used to be traditional to carry the cable screen through the shell of a connector on one of the pins, and connect it to a 0V trace on the PCB, as shown in Figure 3 for an audio product. Many of the standard pin designations for traditional connectors specify one of the pins for the shield, but as Figure 2Y of [5] shows, the resulting ‘pigtail’ screen connection does immense harm to the screen’s RF attenuation.

Figure 3 shows an analogue ‘pro-audio’ product, because I had to use something as an example, and professional audio SNR specifications are very high. I could just have easily used an instrumentation, or even a digital example.

If we assume that the 0V trace is 300mm long and 4mm wide, and is made of 1oz copper, its end-to-end resistance will be about $35\text{m}\Omega$ [12]. Let’s also assume that one of the cable screens is carrying 100mArms of 50Hz ‘earth/ground loop’ current. 100mA in $35\text{m}\Omega$ creates 3.5mV of voltage difference along the 300mm 0V trace, which is used as the reference voltage for the signals in all of the circuits.

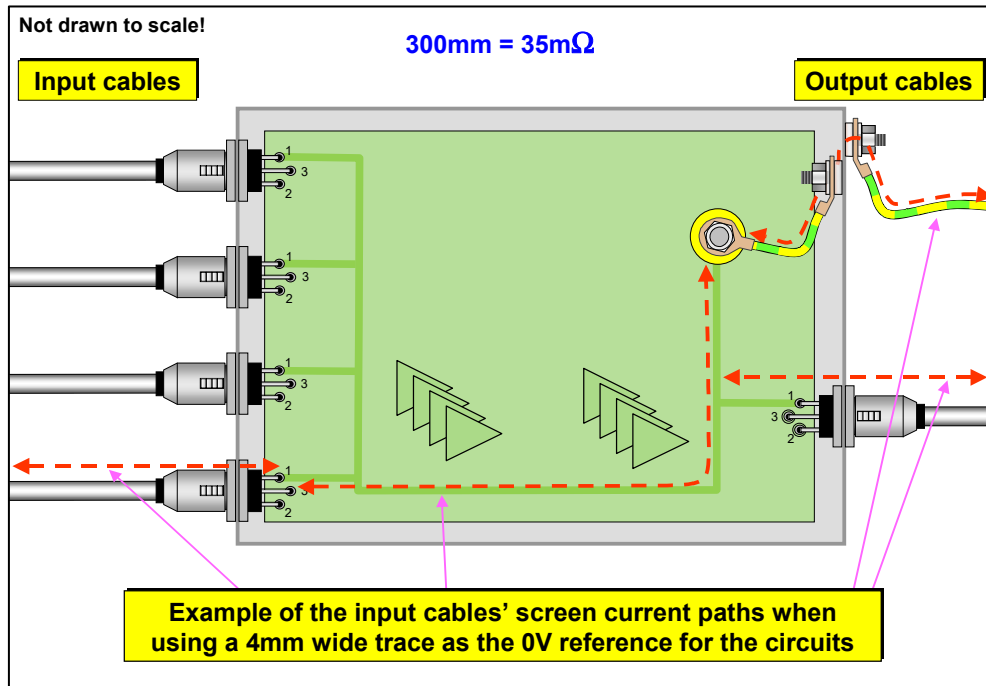


Figure 3 Example of traditional design

If all of this noise voltage appeared in a 10Vrms output signal – as it easily could with such a design – it would cause the signal-to-noise ratio (SNR) to degrade to 69dB (equivalent to a digital resolution of about 11.5 bits).

Now consider the same product with a single PCB over the entire product, with a solid copper 0V plane made from 1oz copper, as shown in Figure 4. [7] tells us that the resistance between two 4mm diameter plane bonds 300mm apart is about $0.8\text{m}\Omega$. The 100mA screen current now causes a voltage drop of $80\mu\text{V}$, which if it all appeared in a 10Vrms output signal would give an SNR of 102dB, equivalent to a digital resolution of about 17 bits. This is 33dB better than when using a 4mm 0V trace, with very little additional BOM cost and a much shorter design cycle.

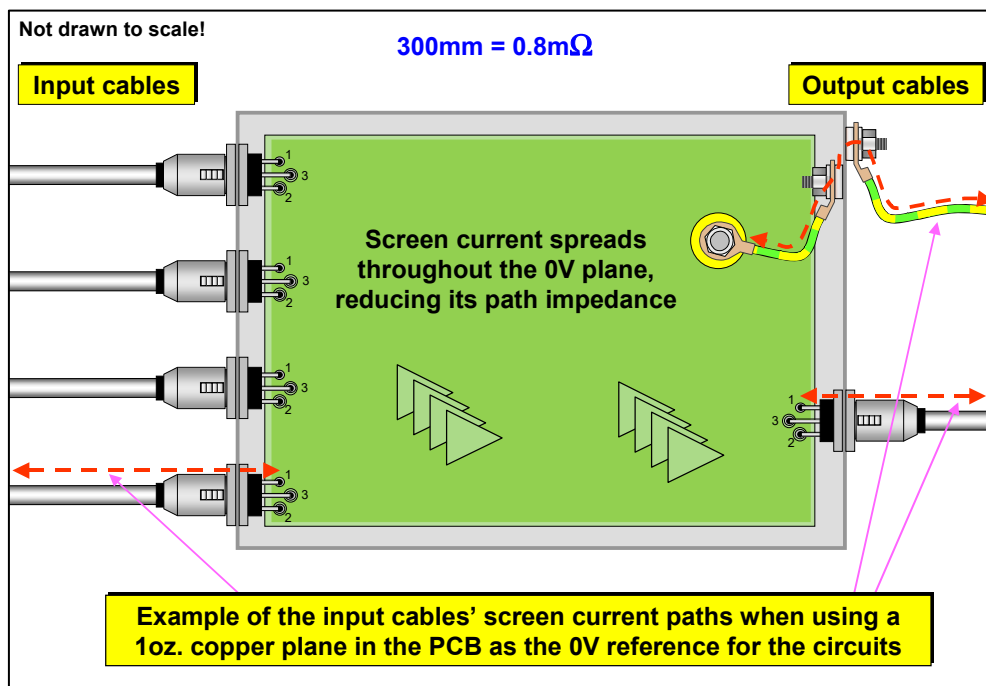


Figure 4 Using a 0V plane instead of a trace

If we now bond the solid copper 0V plane from Figure 4 to the metal chassis of the product, as shown in Figure 5, the resistance of the chassis appears in parallel with that of the plane. If we assume that the chassis is a single plate of 2mm thick aluminium, [7] tells us that between two 4mm diameter bonding points 300mm apart, the resistance is $22\mu\Omega$. With the chassis and the

0V plane effectively connected in parallel, the 100mA screen current now causes a voltage drop of about 2.2 μ V, which if it all appeared in a 10Vrms output signal would have an SNR of 133dB, equivalent to a digital resolution of about 22 bits. This is 31dB better than the 0V plane alone, and 64dB better (more than 1000 times) than when using a 4mm 0V trace, again with very little additional cost.

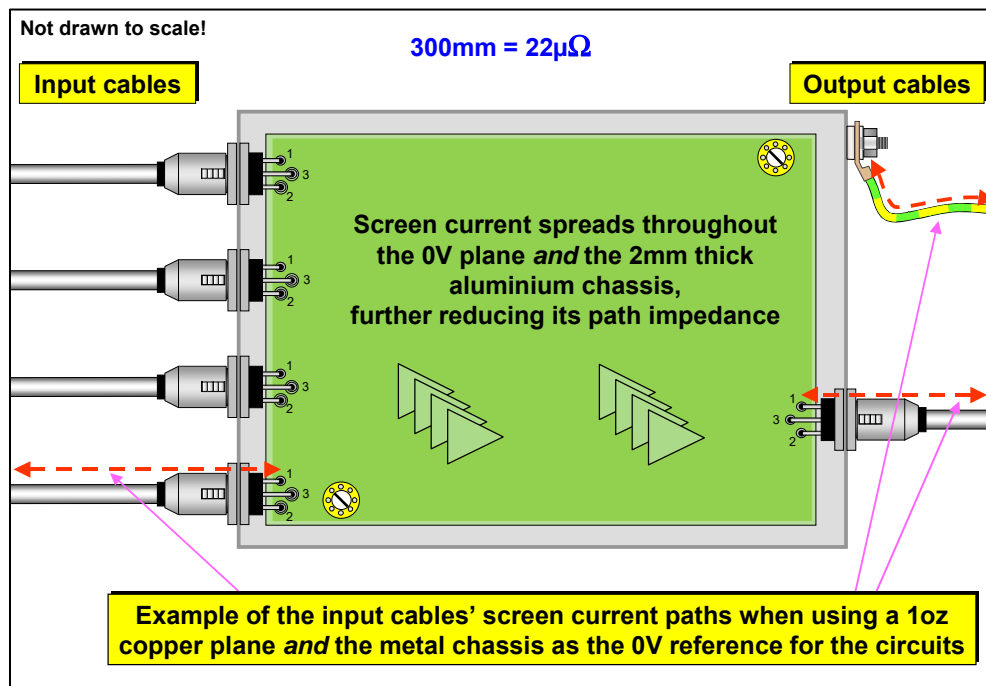


Figure 5 Using a 0V plane bonded to the chassis at two points

Figure 6 shows the same design as Figure 5, but this time with multipoint 0V plane to chassis bonding. We can safely assume that this will improve the SNR by a further 6-10dB at 50Hz. Increasing the chassis to 4mm thick aluminium would gain another 6dB.

If you are wondering about the graphical image I have used for the plane-to-chassis bonds in Figures 5 and 6, see Chapter 3 of [8], especially its Figure 3B.

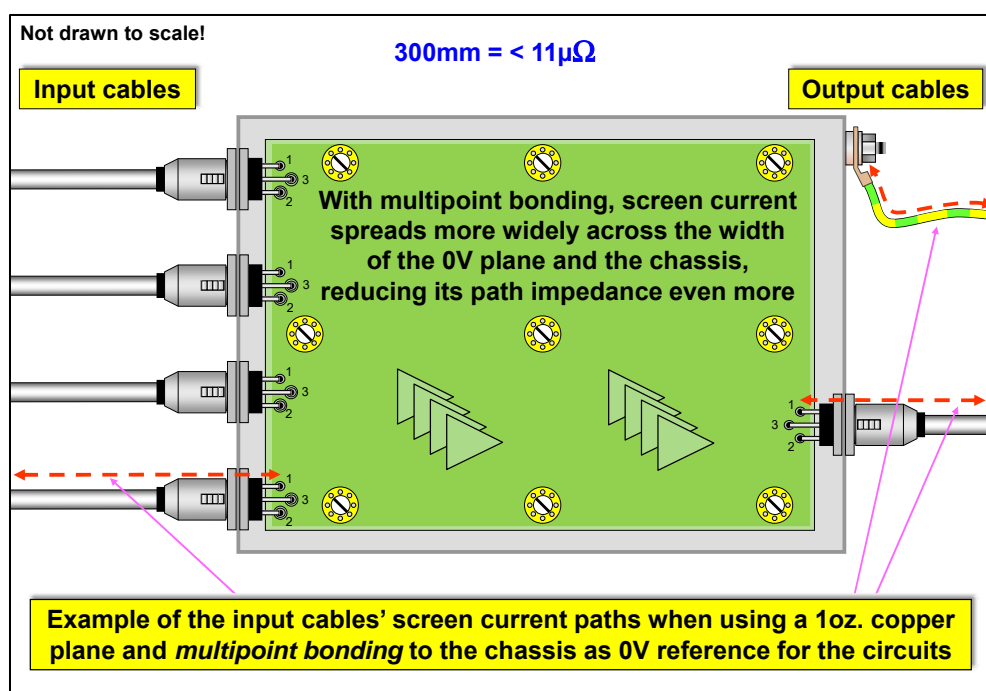


Figure 6 Using a 0V plane multi-point bonded to the chassis

In the above, admittedly rather crude analysis, I simply assumed that the 50Hz 'ground noise' voltage that was developed along the 300mm of 0V current trace on the PCB appeared in the output of a 10Vrms (full scale) signal. But the noise is developed along the length of its 0V current path, so has the characteristics of mV/metre, or $\mu\text{V}/\text{mm}$.

Wherever a circuit uses differential signalling, 'ground noise' in the 0V reference structure appears as CM noise and is attenuated more the higher the CMR. But when using single-ended signalling, it appears as a DM noise *directly in series with the signal*. Understanding that the ground noise appears as $\mu\text{V}/\text{mm}$ helps when deciding where to place components and route traces, so that as little of it as possible gets amplified.

Of course, reducing the impedance of the 0V reference structure in a circuit is not only very good for reducing the noise contributions of cable screen currents, it is also good for reducing the noise contributions from *any* source within the product, leading directly to better signal integrity, SNR, crosstalk, etc.

As I learned in the years up to 1981, very careful design of 0V traces, using 'single-point grounding' techniques, can achieve good control of 50Hz 'ground noise', and crosstalk even up to 20kHz. Some of the artwork for my PCBs were amazing, almost works of art (even if I do say so myself!), and they took a long time to get just right.

But during 1981 I learned that wherever there is modulated RF noise, for instance from a microprocessor or switch-mode power converter anywhere in the product, or entering on cables from outside – the only low-cost technique that can be relied upon to work well for both SNR and crosstalk whilst *reducing* time-to-market, is to use a solid 0V plane layer over the whole PCB. Ideally multi-point bonded to a thick metal chassis. My boards now had four layers, rather than two, and were much quicker to lay out.

Finally, 100mA rms is rather a lot of earth/ground potential equalising current, but might not be that unusual for a long cable with a braid shield in a large installation that had been constructed along 'single-point earthing' rules, when it was the only cable screen bonded at both ends.

But with a meshed earthing structure (MESH-CBN) as recommended by [11], the earth/ground potential differences would be 10 to 100 times smaller – so the effect on SNR of 'ground noise' caused by low-frequency screen currents flowing inside products would be 20-40dB less.

Where there are many cable screens in a system or installation – the more of them that are bonded at both ends, the lower will be the currents flowing in the screens of each one and the less the effect of screen currents on SNR.

Since the source impedance for the earth/ground potential difference is not zero, encouraging currents to flow in cable screens, and mesh-bonding the earthing structure (all recommended by [11]), will significantly reduce the DM noise caused by capacitive imbalance in differential cables. [3] includes some calculations along these lines, for different values of resistance in building earth structures.

Designing products so that screen currents do not upset circuits or worsen SNR is a powerful, easy and low-cost technique that makes systems integration and installation quick and easy. It also improves their functional performance and reliability, and helps considerably with achieving EMC compliance for products and fixed installations, now the law throughout the EU.

References

- [1] Keith Armstrong, “*Terminating Cable Screens (shields)*”, The EMC Journal, Issue 82, May 2009, pages 19 – 23, www.emcstandards.co.uk/terminating-cable-screens-shields
- [2] Keith Armstrong, “*When the Going Gets Tough – Smarter Design Wins (if you think EMC is about complying with the Directive or FCC – think again!)*”, EMC Journal, Issue 81, March 2009, pages 21-24, www.emcstandards.co.uk/when-the-going-gets-tough-smarter-design-wi
- [3] Tony Waldron and Keith Armstrong “*Bonding Cable Shields at Both Ends to Reduce Noise*”, EMC + Compliance Journal, pages 14-27, May 2002, www.emcstandards.co.uk/bonding-cable-shields-at-both-ends-to-reduce-no
- [4] For example, visit:
www.21best.com/21_best/electronic/security/video/filters/for_sale_.html#HBPremium
- [5] Keith Armstrong, “*Design Techniques for EMC, Part 2 – Cables and Connectors*”, www.emcstandards.co.uk/emc-techniques-in-electronic-design-part-2-cabl
- [6] Skin depth: www.rfcafe.com/references/electrical/skin-depth.htm
- [7] Howard Johnson, “Power Plane Resistance”, www.sigcon.com/Pubs/edn/ppresistance.htm
- [8] Keith Armstrong, “*EMC for Printed Circuit Boards – Basic and Advanced Design and Layout Techniques*”, Nutwood, February 2007, ISBN 978-0-9555118-5-1, only available from www.emcacademy.org/books.asp (printed on-demand), or: www.emcstandards.co.uk/basic-and-advanced-design-of-pcbs-series-2004-5
- [9] Keith Armstrong, “*Design Techniques for EMC, Part 4 – Shielding*”, www.emcstandards.co.uk/emc-techniques-in-electronic-design-part-4-shie
- [10] Keith Armstrong, “*Design Techniques for EMC, Part 5 – PCBs*”, at www.emcstandards.co.uk/design-techniques-for-emc-part-5-printed-circui
- [11] BS IEC 61000-5-2:1997, “*Electromagnetic Compatibility (EMC) – Part 5: Installation and Mitigation Guidelines - Section 2: Earthing and cabling*”
- [12] “PCB Trace Resistance Calculator”, at: <http://circuitcalculator.com/wordpress/2006/01/24/trace-resistance-calculator>