

Another EMC resource from EMC Standards

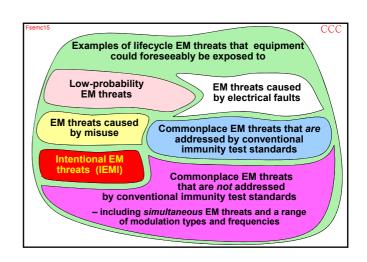
Design & mitigation techniques for EMC for Functional Safety

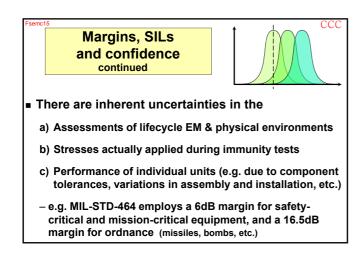


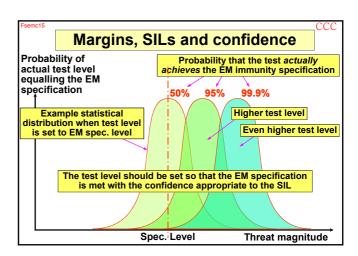
We need to <u>design</u> EMC for safety ■ Where errors or failures in electronics/software could increase safety risks - EM performance must be adequate for the foreseeable worst-case EM environment, over the lifecycle (see my IEEE papers 2001-2003) ■ Proving this by EM testing alone is unfeasible - nobody could afford the time/cost of the test plan - so we need to employ good EM engineering practices

in design and mitigation (see my 2004 IEEE paper)

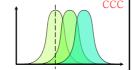
The foreseeable 'worst-case' EM and physical environment(s) should be assessed - to help create the design and test specifications Physical environment(s) should be assessed so EM measures can be designed to last the lifecycle There is usually no data on statistical variations in these environments - so we must design for the foreseeable worst-cases +how to do the necessary EM and physical environment assessments was described in my 2005 IEEE paper







Margins, SILs and confidence continued



- So, when setting the EM specifications that will be used as the basis for the design, and for the verification tests
 - an analysis of the various uncertainties is required
 - and the specified EM threat levels increased by the resulting 'test margin', depending on the SIL required
 - for each cell of the threat/performance matrix (see later)
- A similar approach is required for physical stress tests

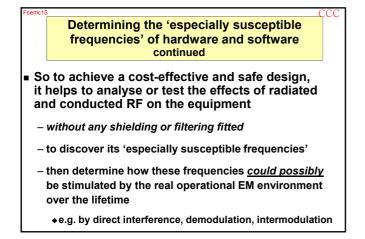
Determining the EM performance criteria

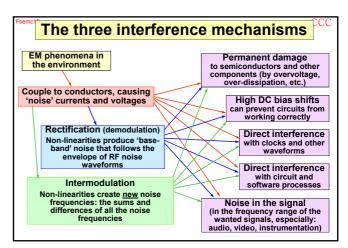
- Different functional safety performance criteria will be required for the various safety functions
 - when they are interfered with by the various EM threats
- So it is necessary to create a matrix of safety functions versus EM threats
 - with the functional performance required specified in the resulting cells
 - note that the usual immunity test performance criteria
 (A, B and C) don't apply we need to know exactly what happens when interference occurs

Example of a threat / performance matrix Function Actuator position error Pressure error Warning siren Must not operate < ±0.1mm < ±0.1% when not required, or fail when required during / after tes during / after tes Must not operate hen *not* required, or 800MHz - 5GHz during / after test during / after test fail when required May operate when < ±1mm not required, must during /after test or fail-safe during /after test or fail-safe not fail when required 2.35 -2.55GHz May operate < 1s upon each surge, during /after test during /after test must not fail when required Etc. Etc. Etc

Determining the 'naturally susceptible frequencies' of hardware and software

- Equipment is especially susceptible at certain 'natural' frequencies, including the
 - full bandwidths of any analogue circuits
 - resonant frequencies of cables, metal structures, transducers or actuators
 - digital clock frequencies, sampling rates,
 RF carrier and modulation frequencies
 - ◆and all of their harmonics





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Determining the 'especially susceptible frequencies' of hardware and software continued

- Intermodulation occurs in all semiconductors, and at all corroded electrical joints (known as the 'rusty bolt effect')
 - an important lifecycle consideration
 - (normal EMC RF testing uses single frequencies, so doesn't test intermodulation possibilities)
- To prevent demodulation and intermodulation from causing immunity problems in real life
 - it may be necessary to shield and filter at frequencies well beyond the 'especially susceptible frequencies'

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Coping with foreseeable faults

- Faults can include
 - ◆components open/short circuited, or altered parameters
 - ◆broken electrical bonds (e.g. shield joints, filter grounding)
 - ◆increased impedance at shield gaskets, etc.
 - appropriate design for the foreseeable physical environment can reduce likelihood of most faults
- Where a fault can lead to a safety risk, IEC 61508 describes design techniques for achieving the SIL
 - ◆e.g. duplication, triplication, etc.
 - ◆e.g. condition monitoring with safety shut-down, etc.

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EMI mitigation when using multiple redundant channels

- EMC is a systematic (common cause) failure
 - so, where IEC 61508 requires multiple channels to meet the SIL, the use of <u>diverse technologies</u> is required
- But using multiple diverse-technology channels doesn't mean each can have low EM performance
 - otherwise, during interference, it could happen that none of the digital channels would function correctly
 - ♦ and all the analogue channels could be at + / full scale
 - ♦ (a similar issue for common-cause physical threats too)

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Interference sensing techniques

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- Interference sensors can be used inside or outside equipment
 - to detect EM events which might cause hazards
 - and initiate special protective measures or shut-down the equipment safely
 - ◆e.g. used to protect some military equipment from the pulses caused by nuclear explosions
 - e.g. used by gaming machine manufacturers to protect them from people trying to 'break' the machine with interference (e.g. using cattle prods)

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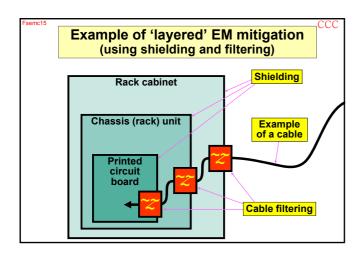
Interference sensing techniques continued...

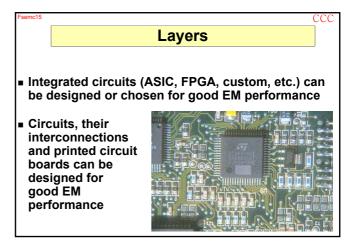
- A safety interlock on a door or panel can tell if it has been opened
 - and inhibit the equipment so as to protect people from the possible safety consequences of degraded shielding
 - treating the door like a machine guard that interlocks with an emergency stop function
- But EM sensors can detect accidentally degraded shielding or filtering, or unforeseen EM threats
 - and could allow doors to be opened without protective shut-down (unless EM threats are present)

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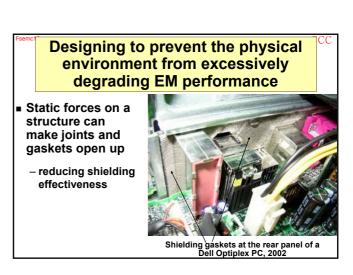
A 'layered' approach to EM mitigation

- It is often less costly, and more reliable, to use a number of 'layers' of EM mitigation
 - rather than relying on a single 'layer'
 - ◆e.g. high-performance shielding and filtering of the equipment's enclosure
- It is recommended to design so that if one 'layer' should fail completely for some <u>unforeseen</u> reason
 - ◆e.g. misuse, whether accidental or intentional
 - the equipment will still have adequate EM performance



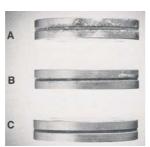


Layers continued... ■ Fibre-optic cables preferred for signal and control - or else cables should carry serial digital data protected by a proven robust error correcting protocol (e.g. '1553') ■ Shielding, filtering, surge, transient, and ESD protection can be applied at the following levels... • individual devices • printed circuit assemblies • modules and sub-assemblies • units (e.g. rack mounted equipment) • overall enclosure level (e.g. rack cabinets) • and even to rooms, buildings, and sites (campuses)





- Repetitive stress, shock, vibration, oxidation and corrosion can cause
 - wear-out of joints / gaskets
 - gaps in cable shields
 - loosened fixings
 - open / short circuits in conductors and component leads
 - connectors to work loose



Results of a test comparing lifetime corrosion for three different types of shielding gaskets

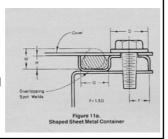
EMC problems caused by the physical environment continued...

- These physical effects can ruin shielding effectiveness
- They can also cause filters to become less effective
 - ◆e.g. by breaking their ground connections
 - with similar problems for surge, transient and ESD protective devices
- And they can make circuits on PCBs unstable
 - ♦ much more prone to causing or suffering EMI

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Protecting from foreseeable "physical EMC problems"

- The equipment <u>must</u> be designed so that its EM performance remains sufficient over its lifecycle
 - despite all foreseeable physical stresses, wear and ageing
- Mechanical structures may need to be designed for forces, shock and vibration with the aid of finite element analysis





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Preventing degraded EM performance from foreseeable use (or misuse)

- Installation, commissioning or maintenance instructions might not be followed
 - so it is best if these tasks are done by the manufacturer
- Users might open doors, covers or panels when they shouldn't, or make unapproved modifications
 - so we must anticipate what could foreseeably happen, then design, guard and warn accordingly (in that order)
 - ◆ sometimes users will need to be trained, maybe even pass an exam, before being appointed a "keyholder"

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EM design/mitigation techniques in system integration/ installation

■ Good EM practices should be employed during

 cable segregation and routing earthing and mesh-bonding shielding filtering

and other publications

transient suppression

• these are described in IEC 61000-5-2 and -6

installation, including techniques for

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QA procedures should control

- Design reviews (independent experts may be required)
- The exact build state that will achieve the EM performance
- The EM performance of suppliers and subcontractors
- Installation, user and maintenance manuals
 - that clearly describe all that should be done to achieve the required EM performance and maintain it over the lifecycle
- The maintenance of EM performance despite upgrades and modifications



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Some useful references

- Assessing an Electromagnetic Environment Keith Armstrong, downloadable from the "Publications and Downloads" page at http://www.cherryclough.com <u>Note:</u> this was written to help with EMC compliance, not for safety purposes
- The Case for Combining EMC and Environmental Testing, W H Parker, W Tustin, T Masone, ITEM 2002 pp 54-59, www.rbitem.com
- Combined Effects of Several, Simultaneous, EMI Couplings"
 Michel Mardiguian, 2000 IEEE International Symposium on EMC,
 Washington D.C., August 21-25 2000, ISBN 0-7803-5680-2, pp. 181-184
- EMC Performance of Drive Application Under Real Load Condition", F Beck, J Sroka, Schaffner EMV AG application note, 11th March 1999
- Robust Electronic Design Reference Book, Volumes I and II, John R Barnes, Kluwer Academic Publishers, 2004, ISBN: 1-4020-7739-4
- Design Techniques for EMC, Keith Armstrong, EMC Compliance Journal, 1999, www.compliance-club.com/KeithArmstrongPortfolio

Some useful references continued...

- Advanced PCB Design Techniques for EMC, Keith Armstrong, EMC Compliance Journal 05, www.compliance-club.com/KeithArmstrongPortfolio
- EMC for Product Designers, 3rd edition Tim Williams, Newnes, 2001 ISBN 0-7506-4930-5
- EMC for Systems and Installations, Tim Williams and Keith Armstrong, Newnes 2000, ISBN 0-7506-4167-3
- EMC for Systems and Installations Keith Armstrong, EMC Compliance Journal, 1999, www.compliance-club.com/KeithArmstrongPortfolio
- The Design of Military Equipment Enclosures to Minimise the Effects of Corrosion, John Terry, EMC-UK 2005, Newbury, Oct 13-14, pp 85-88
- EMC and Electrical Safety Design Manuals, York EMC Services, 2002, sales@yorkemc.co.uk, phone: +44 (0)1904 434 440

Volume 1 - What is EMC? ISBN 1-902009-05-3 Volume 2 - EMC Design Techniques - Part 1 Volume 3 - EMC Design Techniques - Part 2 Volume 4 - Safety of Electrical Equipment ISBN 1-902009-06-1 ISBN 1-902009-07-X ISBN 1-902009-08-8

Some references for safetyrelated software

- IEC 61805-3: Functional safety of electrical, electronic and programmable electronic safety-related systems Software Requirements
- Development Guidelines for Vehicle Based Software, The Motor Industries Software Reliability Association (MISRA), MIRA Ltd, 1994, ISBN 0 952 41560 7, http://www.misra.org.uk
- Guidelines for the Safety Analysis for Vehicle Based Software, MISRA, MIRA Ltd, 2006, http://www.misra.org.uk
- Noise, EMC and Real-Time, MISRA Report 3, February 95. MISRA, MIRA Ltd, http://www.misra.org.uk
- EMC-Hardening Microprocessor-Based Systems
 Dr D R Coulson, IEE Colloquium "Achieving Electromagnetic
 Compatibility: Accident or Design", 16th April 97, IEE Colloquium Digest: 97/110, sales@iee.org.uk

Some references for safety-related software continued..

Electromagnetic Compatibility of Software, IEE Colloquium, Thursday 12th November 98, IEE Colloquium Digest: 98/471, sales@iee.org.uk

NOTE: The software techniques described in the three references below are equally valuable for improving software immunity to all transients, the main causes of EMC problems for software

- John R Barnes, Designing Electronic Equipment for ESD Immunity, Printed Circuit Design, vol. 18 no. 7, July 2001, pp. 18-26, http://www.dbicorporation.com/esd-art1.htm
- John R Barnes, Designing Electronic Equipment for ESD Immunity Part II, (Printed Circuit Design, Nov. 2001) http://www.dbicorporation.com/esd-art2.htm
- John R Barnes, Designing Electronic Systems for ESD Immunity, Conformity, Vol. 8 No. 1, February 2003, pp. 18-27, http://www.conformity.com/0302designing.pdf

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