Another EMC resource
from EMC Standards

Cost-Effective use of HDI PCB technology for SI, PI and EMC

Helping you solve your EMC problems

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Cost-Effective Use of HDI (microvia) PCB Technology for SI, PI and EMC

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High Density Interconnect (HDI) PCB manufacturing technology

- Also known as microvia technology, or Sequential Build-Up technology (or simply 'Build-Up')…
  - uses 'microvias' 6 thou (0.15mm) diameter or less, so can achieve twice the number of pins/area than THP…
  - and which only connect between necessary board layers, so don't constrain routing on other layers
- All of which means they can significantly reduce the number of PCB layers required…
  - *especially* where THP would require 10 layers or more

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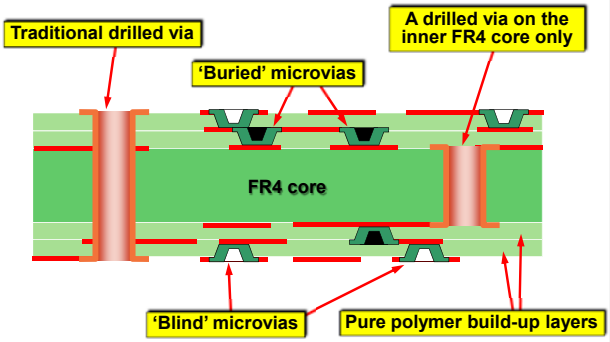
Features of original HDI technology



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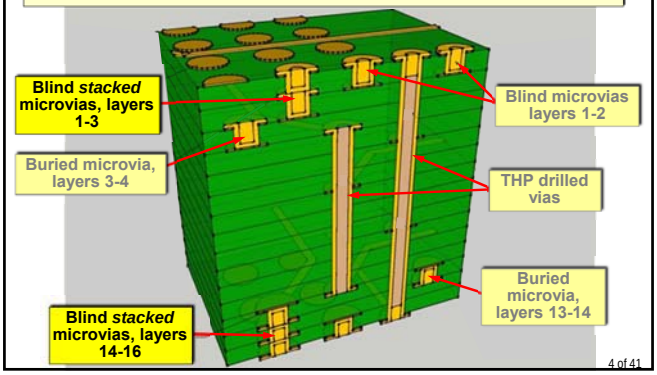
Modern HDI can 'stack' vias

http://designinthetrenches.com/wp-content/uploads/2012/04/HDI21.png



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Microvias are closed at one end…

- so don't steal solder during reflowing, allowing *via-in-pad* layouts…
  - good for EMC because this reduces the inductances associated with power supply decoupling
- But if blind microvias-in-pads are not completely filled/capped to provide a planar copper surface…
  - solder paste printed over them traps little air bubbles…
  - which expand and 'pop' during soldering, possibly causing poor solder joints

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HDI benefits

- HDI techniques help to make the smallest, lightest, and least power-hungry products…
  - and can be found in a wide variety of common products (including some toys)
- Microvias are inherently more robust than THP…
  - so are preferred in some hi-reliability or harsh environment applications

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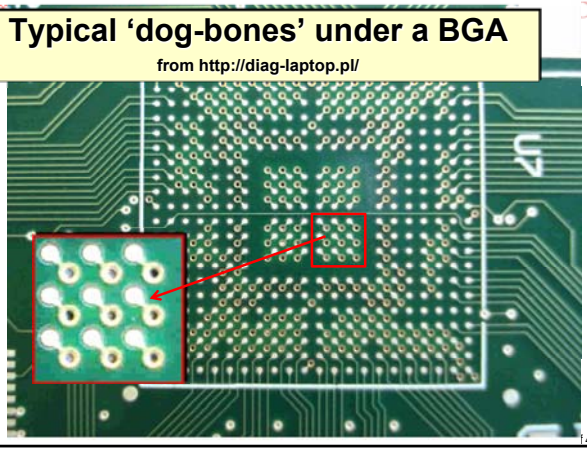
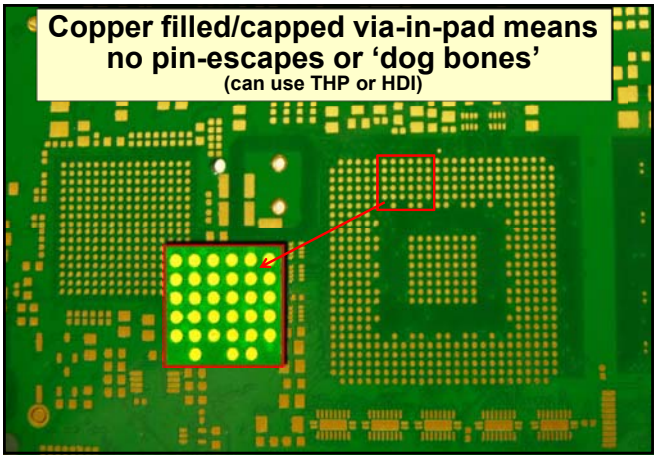
Typical 'dog-bones' under a BGA

from http://diag-laptop.pl/

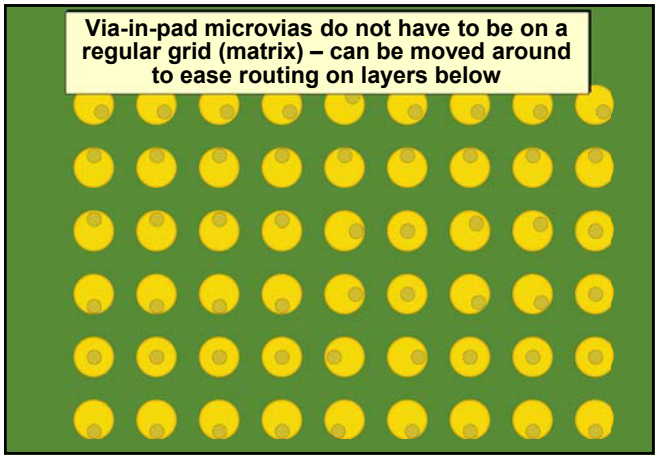


Copper filled/capped via-in-pad means no pin-escapes or 'dog bones'

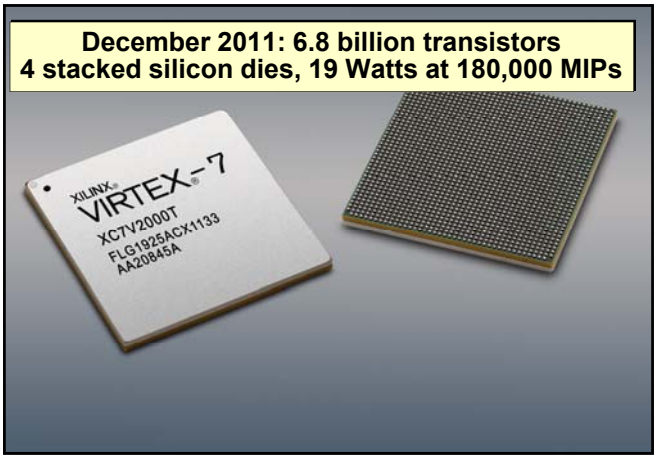
(can use THP or HDI)



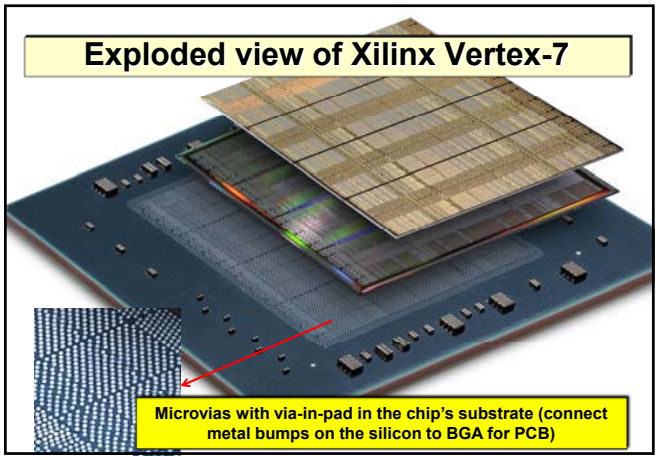
Via-in-pad microvias do not have to be on a regular grid (matrix) – can be moved around to ease routing on layers below



December 2011: 6.8 billion transistors 4 stacked silicon dies, 19 Watts at 180,000 MIPs



Exploded view of Xilinx Vertex-7



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BGA's PI & SI suffers from perforation of the 0V, Power planes underneath

- The best that can be done with THP is to use suitable track-and-space (track-and-gap) layout rules…
  - to try achieve a complete mesh or grid over the area covered by the BGA's solder pads…
    - as discussed in my previous Webinar, on June 25, 2014

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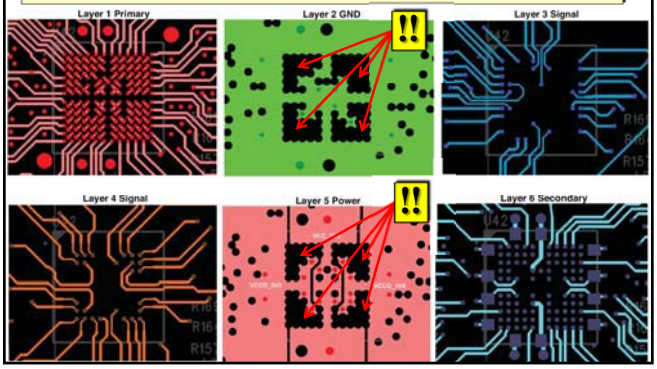
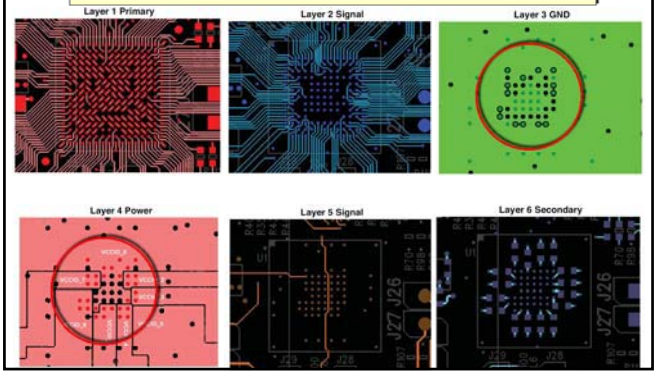
Example of poor plane meshing under BGAs

from: '*Figure 18-8. CAM Artwork Screen Shots, Example #1, 144-ball csBGA*', Lattice Semiconductor Technical Note TN1074: 'PCB Layout Recommendations for BGA Packages', Sept. 2013



Example of good plane meshing under BGAs

from: '*Figure 18-10. CAM Artwork Screen Shots, Example #1, 256-Ball caBGA*', in Lattice Semiconductor Technical Note TN1074: 'PCB Layout Recommendations for BGA Packages', Sept. 2013



HDI 0V planes aren't perforated…

- and so create solid, continuous 0V/Power plane pairs under BGAs, with lower series inductances, higher mutual inductances and higher capacitances which all improves decoupling…
  - improving both PI and EMC
- and they provide lower and more constant return path inductances…
  - improving both SI and EMC

- **Where microvias *do* perforate a plane, the gaps they create are very small…**
  - so the effects on SI, PI and EMC are small

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HDI's additional EMC benefits include…

- via-in-pad reduces decoupling inductances, pushing PDN resonances to higher frequencies…
- shorter traces become efficient 'accidental antennas' at higher frequencies…
- smaller PCBs become efficient "accidental patch antennas" at higher frequencies…
- shorter traces may not need to be treated as transmission lines…
- less perforated 0V and Power planes have improved 'image plane' effect so have higher shielding effectiveness

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Poll Questions

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HDI makes it possible to use the smallest IC package styles, and obtain their EMC benefits, e.g…

- Miniature or Micro BGA (especially with ball pitch <1mm)
- DCA (direct chip attach)
- Flip-chip
- CSP (chip scale packaging)
- TAB (tape automated bonding)

- **These very small, thin semiconductor packages have much closer proximity to the PVB's 0V/Power planes than a regular packaged IC…**
  - so their 'image plane' effect is stronger – reducing emissions, and increasing immunity

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Beware, when using chip-scale package styles!

- Because they lack the inductances associated with bond wires and lead-frames…
  - their very sharp internal switching speeds 'leak' higher levels of higher frequency noises into the PCB structure, making EMC worse…
  - unless HDI and good EMC design techniques are used

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HDI suppliers and technologies

- In May 2000 there were 62 manufacturers of HDI boards worldwide, and in May 2008 there were 32 manufacturers just in the UK…
  - their manufacturing techniques can vary, and may need different layout techniques, so always check with chosen manufacturer *before* starting board layout
- Basic standard: IPC-2315 (from www.ipc.org)…
  - some good EMC PCB design techniques were made impractical by *original* HDI technology…
    - e.g. 0V/Power plane pairs adjacent to top/bottom sides…
  - made practical again by modern microvia technologies

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HDI costs

- An IPC survey in 2000 found HDI boards could be purchased for the same cost as THP…
  - and not using buried vias helps reduce costs further
- Latest advice (Mentor Graphics) is that boards needing > 8-10 layers should *cost less* if made in HDI…
  - e.g. a high-density 18 layer THP board would only need 10 layers if using HDI…
    - but even for lower densities or fewer layers, HDI's EMC, SI and PI advantages make it more cost-effective than THP…
  - focussing on the BOM cost instead of 'overall cost of manufacture' is a common management mistake!

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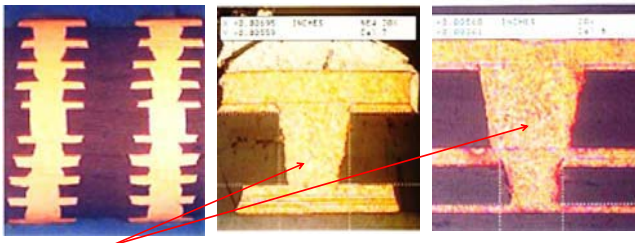
Some *modern* microvia technologies

(these ones are from Viasystems, visit: www.viasystems.com/technology/hdi.html)

1) Stacked or Second Generation MicroVias (SMV®)

2) Deep Microvias (DpMV™)

3) Deep Stacked MicroVias (DpSMV™)



These types claimed to provide a planar surface for via-in-pad BGAs, and have improved current capacity & thermal management

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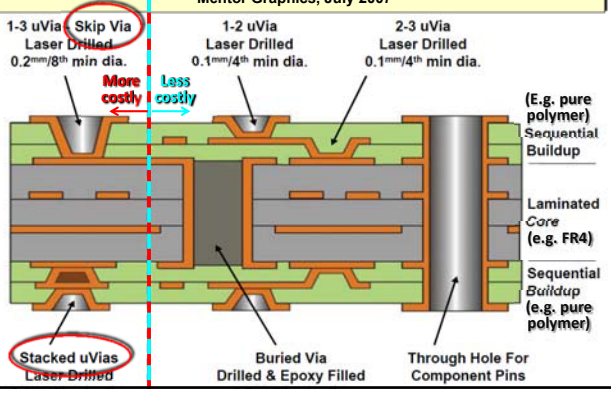
More examples of modern microvia techniques

'HDI Layer Stackups for Large Dense PCBs', Happy Holden & Charles Pfeil, Mentor Graphics, July 2007



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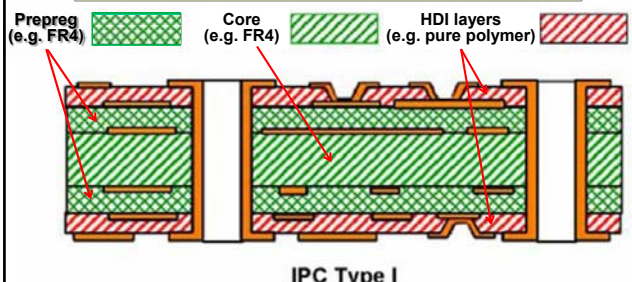
HDI construction: 'IPC Type I'

from "HDI Layer Stackups for Large Dense PCBs", by Happy Holden and Charles Pfeil, Mentor Graphics, July 2007

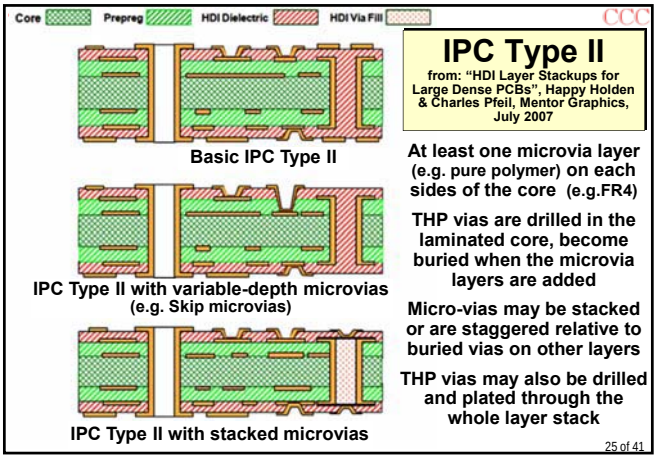


IPC Type I

IPC Type I has microvias & THP vias, and laminated core (e.g. FR4) with a *single* microvia layer (e.g. pure polymer) *on at least one side*
Note: no buried THP vias

IPC Type II

from: "HDI Layer Stackups for Large Dense PCBs", Happy Holden & Charles Pfeil, Mentor Graphics, July 2007



At least one microvia layer (e.g. pure polymer) on each sides of the core (e.g.FR4)

THP vias are drilled in the laminated core, become buried when the microvia layers are added

Micro-vias may be stacked or are staggered relative to buried vias on other layers

THP vias may also be drilled and plated through the whole layer stack

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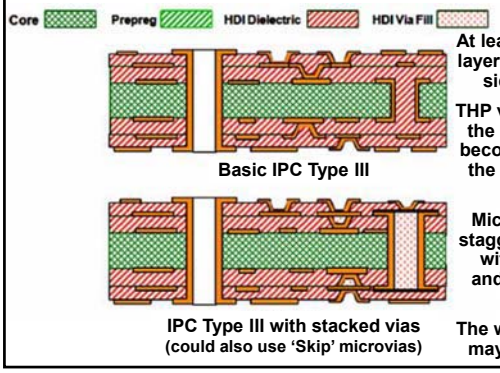
IPC Type III

from: "HDI Layer Stackups for Large Dense PCBs", Happy Holden & Charles Pfeil, Mentor Graphics, July 2007



At least two micro-via layers on at least one side of the core

THP vias are drilled in the laminated core, become buried when the microvia layers are added

Micro-vias may be staggered or stacked with themselves and/or with buried THP vias

The whole layer stack may have THP vias

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Some HDI stack-up issues

- **IPC Types I, II and II use a core (e.g. FR4) with FR4 or polymer 'build-up' layers containing microvias and/or THP vias, to keep costs low…**
  - **but different layer materials have different temperature coefficients and rates of moisture absorbance…**
    - **so delamination is a real possibility, especially if there is significant temperature and/or humidity cycling…**
  - **not a problem, of course, when using same material for every layer**
- ***Some people say:* "IPC Type IV, V, VI HDI constructions are more costly, and probably not necessary for large dense PCBs with BGA breakout and routing challenges"**

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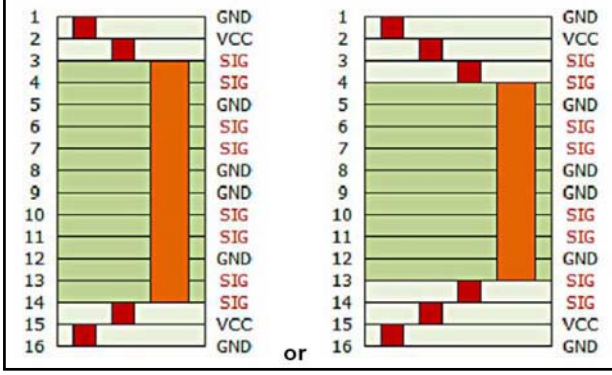
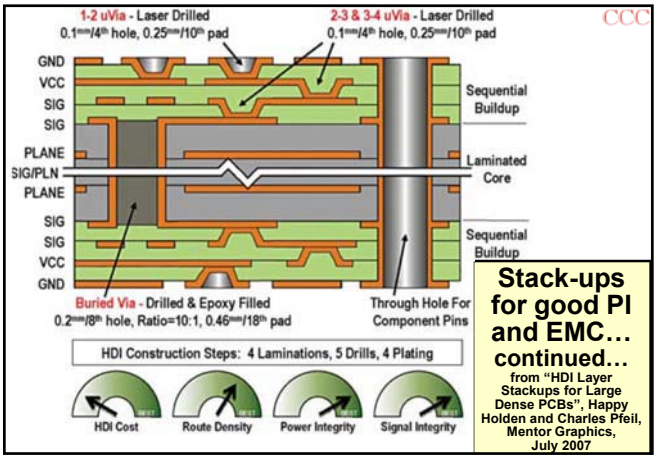
Stack-ups for good PI and EMC

from "HDI Layer Stackups for Large Dense PCBs", by Happy Holden and Charles Pfeil, Mentor Graphics, July 2007





Stack-ups for good PI and EMC… continued…

from "HDI Layer Stackups for Large Dense PCBs", Happy Holden and Charles Pfeil, Mentor Graphics, July 2007

Stack-ups for good PI and EMC continued...

- **Top and Bottom layers as 0V (i.e. GND) planes helps shield all the internal traces…**
  - **with perimeter guard traces and low-cost BLS (board level shields) can make fully-shielded PCB assemblies…**
    - **see my PCB book for more details…**
  - **usually 30% or more BGA pins are 0V and many of the rest are Power, but microvia antipads are very small…**
    - **so the perforation of these planes is not very great**
- **Power (VCC, VDD) planes on adjacent layers create distributed (embedded) decoupling capacitances immediately below the devices: best for PI**

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Stack-ups for good PI and EMC continued...

- **These stackups benefit from stacked microvias, and board size, product weight/size, and overall manufacturing costs can be reduced by:**
  - **embedded pull-up and termination resistors…**
  - **embedded surge/transient protection…**
  - **embedded ICs (like smart cards)…**
  - **embedded decoupling capacitors…**
  - **embedded high-capacitance laminates ideally less than 50µm (0.002 inch) thick between 0V/Power planes, can provide several nF per square centimetre, making it possible to eliminate all soldered decoupling capacitors (excluding 'bulk' caps ≥ 10µF)**

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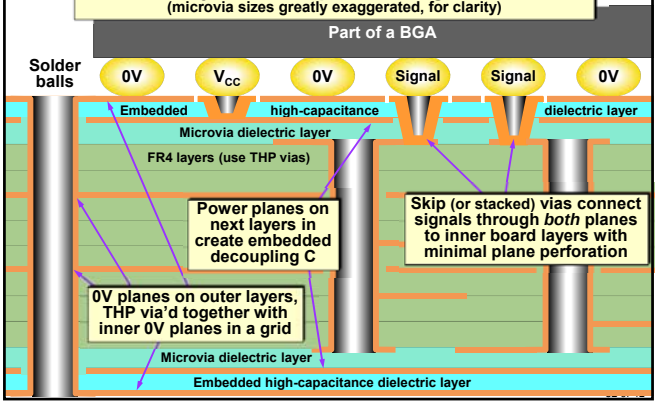
Example of a good construction for PI & EMC by Lode Decapmaker, Belgium

(microvia sizes greatly exaggerated, for clarity)



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the end

interference technology

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Poll Questions

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Some useful sources for HDI (microvia)

- *HDI Technology Moves Into Mainstream Design*, H Holden, Printed Circuit Design & Manufacture, Dec 06, www.pcdandm.com/cms/images/stories/mag/0612/0612pcdm_digital.pdf
- *HDI's Beneficial Influence on High-Frequency Signal Integrity, Parts 1 and 2*, H Holden, http://www.mentor.com/pads/techpapers
- *HDI and Microvia Technology*, www.ipc.org/html/hdi.htm (includes > 25 useful articles)
- *Planning, Predictive Engineering, and DFM for Advanced Circuit Boards*, H. Holden, PCB Design Conference West, March 1999
- *PWB Microvia Costs: Objective Guidance for Today's Decision-Making* Adam Singer, Ravi Bhatkal, Jack Fisher; IPCWorks 1997

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Some useful sources for HDI (microvia) continued…

- IPC-2315, "*Design Guide for High Density Interconnects & Microvias*", and a number of other standards and guides on HDI, Build-up, and Microvia PCB technology, including IPC-2226, IPC-4104, IPC-6016 and IPC-9151, can be purchased on-line from IPC at www.ipc.org
- "*HDI's Beneficial Influence on High-Frequency Signal Integrity, Parts 1 and 2*", Happy Holden, available via Mentor Graphics' index: www.mentor.com/techpapers/fulfillment (search for HDI)

  or direct from:
  www.mentor.com/products/pcb-system-design/techpubs/hdi-s-beneficial-influence-on-high-frequency-signal-integrity-part-1-7404, *and:*
  www.mentor.com/products/pcb-system-design/techpubs/hdi-s-beneficial-influence-on-high-frequency-signal-integrity-part-2-7405

  (many other good HDI papers from Mentor Graphics' index: search by 'HDI')

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Some useful sources for HDI (microvia) continued…

- "*Signal Integrity and HDI Substrates*", Dr Eric Bogatin, The Board Authority, Vol 1(2), A supplement to Circuitree Magazine, June 1999, page 22, available via the list of articles and technical papers at www.bethesignal.com, or direct from www.bethesignal.net/bogatin/bts022-signal-integrity-p-167.html?cPath=23
- "*Cost-Effective Use of Microvias*", Charles Capers, Printed Circuit Design, March 2003, Vol. 20 Issue 3, p14, http://connection.ebscohost.com/c/articles/9223337/cost-effective-use-microvias
- "*Microvias and RF – ready for 10GHz?*", Ron Neale, Editor, Electronic Engineering, August 2000 pp 59-62, https://getinfo.de/app/Microvias-and-RF-ready-for-10GHz/id/BLSE%3ARN082408538
- "*The Via Squeeze*", Charles L Lassen and Mark V Christensen, IEEE Spectrum, Volume 36, Issue 10, October 1999 pp 36, 38-41, ieeexplore.ieee.org/iel5/6/17247/00795606.pdf

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Some useful sources for HDI (microvia) continued…

- "*Deep Microvias in Next Generation System Design*", Leigh Eichel, International Cadence Users Group Conference 2003, www.amphenol-tcs.com/doc?id=36 (may also be available via: www.teradyne.com/prods/tcs/resource_center/whitepapers.html)
- "*How To Get Started in HDI With Microvias*", Happy Holden, Mentor Graphics Technical Paper Series, www.mentor.com/pcb/resources/overview/how-to-get-started-in-hdi-with-microvias-6c012699-5d73-4596-aeec-0ce7de663a3d
- "*Printed Circuits Handbook*", by Clyde Coombs, Edition 6, October 2007, ISBN: 9780071467346, https://www.mcgraw-hill.co.uk/html/0071467343.html
- "*Solutions Beyond Limits*" Viasystems Group, Inc., IPC Northwest Design Council , July 26, 2012, http://dcchapters.ipc.org/assets/pnw/presentations/20120726_microbga.pdf

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Some useful sources for HDI (microvia) continued…

- "*The HDI Handbook*", by Happy Holden, John Andresakis, Eric Bogatin, et al, www.hdihandbook.com
- "*Power Integrity Effects of High Density Interconnect (HDI)*", by Happy Holden, available from Mentor Graphics' index at www.mentor.com/techpapers/fulfillment (search for HDI) or direct from: www.mentor.com/pcb/resources/overview/power-integrity-effects-of-high-density-interconnect-hdi--a4c6125f-12b7-4a4d-9d51-1323cc4a8552 (many other good HDI papers from this Mentor Graphics index: search by 'HDI')
- "PCB Layout Recommendations for BGA Packages", Lattice Semiconductor Technical Note TN1074, September 2013, www.latticesemi.com/~/media/Documents/ApplicationNotes/PT/PCBLayoutRecommendationsforBGAPackages.pdf?document_id=671
- "Microvias in Printed Circuit Design", Kevin Arledge and Tom Swirbel of Motorola Land Mobile Products Sector, www.eetasia.com/ARTICLES/2000FEB/2000FEB24_SMT_ICP_AN.PDF?SOURCES=DOWNLOAD

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Some useful sources for HDI (microvia) continued…

- "*HDI and Advanced HDI*", Viasystems Group, Inc., www.viasystems.com/technology/hdi.html
- "*HDI Layer Stackups for Large Dense PCBs*", by Happy Holden and Charles Pfeil, Mentor Graphics, July 2007, http://communities.mentor.com/mgcx/servlet/JiveServlet/downloadBody/1128-102-1-1183/hdi%20_layer_stackups_for_large_dense_pcbs.pdf
- "*HDI Printed Circuit Boards*", NCAB Group, www.ncabgroup.com/wp-content/uploads/2012/01/hdi_presentation_110913.pdf
- "*HDI*", by Kenneth Jonsson and Bo Andersson, NCAB Group, www.dnu.no/arkiv3/HDI%20-IPC%20presentation_Norge%20090924-2.pdf
- "*Multi-Chip Module*". http://en.wikipedia.org/wiki/Multi-chip_module
- "*Package on Package*", http://en.wikipedia.org/wiki/Package_on_package

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Some useful sources for embedded/buried PCB components

- "*PCBs With Embedded Components Emerge for Capacitors*", introduces the GRU series of embedded capacitors, www.murata.com/products/article/pdf/ta10d1.pdf
- "*Shocking Rules and Material Remove ESD Risk in Allegro PCB Smartphone Designs*", by Team Allegro on June 27, 2012, www.cadence.com/Community/blogs/pcb/archive/2012/06/27/shocking-rules-remove-esd-risk-in-allegro-pcb-smartphone-designs.aspx
- "*Faradflex*" from Oak-Mitsui, www.faradflex.com, and www.oakmitsui.com/pages/advancedtechnology/faradflex.asp
- "*Buried Capacitance® Technology*", www.sanmina.com/pdf/solutions/pcbres/buried_capacitance_technical_0106.pdf, and www.sanmina.com/pdf/solutions/bc.pdf

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Some useful sources for embedded/buried PCB components continued…

- "*Reduce PCB Impedance, Noise, and EMI and Simplify PCB Layout*", describes 3M™ Embedded Capacitance Material (ECM), http://solutions.3m.co.uk/wps/portal/3M/en_GB/EmbeddedCapacitanceMaterial/Home/
- "*Plated Additive Resistor Technology*", describes MacDermid's 'M-Pass' resistive layer technology, http://aept.ncms.org/presentations/09%20MacD%2001'30'2003.pdf
- *"Embedded Passives: Debut in Prime Time"*, by Joel S. Peiffer, http://pcdandf.com/cms/component/content/article/220-2009-issues/6786-embedded-passives-debut-in-prime-time

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Other useful sources

- **Fully-shielded PCB assembly, see: "*EMC for Printed Circuit Boards, Basic and Advanced design and layout techniques*", Edition 2, Nutwood UK December 2010, ISBN 978-0-9555118-5-1, full colour graphics throughout, from www.emcacademy.org/books.asp**

  ***not** available via Amazon or other distributors*, **who might indicate that it is out of print when in fact it is printed on demand. This 2nd Edition is identical to the 1st Edition except for size/format – if you have the 1st Edition, no need to buy the 2nd !**

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