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| **Draft Checklist of Good EM Engineering Practices for Electronic Products, with references for obtaining more detailed information**All of the following sections cover both emissions and immunity, unless stated otherwise*(Please note: This checklist was created in 2012 and has not been updated since, so should be considered to be a first draft)(It is provided in Word format so that it is easy to adapt/cut/paste/etc. into your own documentation formats and styles.)* This checklist should be treated as a starting point for good EMC design that will save time and cost and improve profitability, because good EMC design is also excellent design for SI and PI (see chapter 1.1 in [1]). The two books referenced above contain much more guidance on good EMC design techniques than can be included in a practical checklist, and both may *only* be purchased from www.emcacademy.org/books.asp. Keith Armstrong’s “Cost-Effective EMC Design” training courses are kept up to date and will therefore include additional material to what is included in these books.**Acronyms**SI Signal Integrity (for analogue and digital signals, data, control, etc.)PI Power Integrity (for the DC power rails supplied to the circuits)EMC ElectroMagnetic Compatibility, the compatibility between a product’s emissions and immunity and its electromagnetic environment.DM Differential Mode – the mode of propagation of the wanted power/signals/data, which can also suffer from noiseCM Common Mode – the mode of propagation of noises caused by imbalances in physical constructions and circuits, usually having much more significance for emissions and immunity at frequencies above 1MHz than DM THP Through Hole Plate, the usual was of manufacturing PCBs at this time, where the etched copper layers are stacked and laminated together, and connections made between layers by drilling right through the and plated the barrels of the holes thus formed.  The wavelength of the frequency *f*, calculated for air as  = 300/*f* . *f* in MHz gives  in metres. *f* in GHz gives  in millimetres.The wavelengths associated with fibreglass PCB traces are about half of what they are in the air, and for alumina or glass substrates they are about one-third.  |
| **Space for project name, number, etc.** (all the relevant details for traceability) |
| **Space for author’s name, date created, version number, change control, etc.** |

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| Project management and system design |
| **Good EM Engineering Practice** | **References** | **How applied**(Whether applied or not, also how applied, with justifications and any references to other documents) |
| 1.1 | List all the EMC standards which are relevant (e.g. for the EU, USA, other countries), and state whether their testing is required in each case. | [1] 1.3 |  |
| 1.2 | Check to see if there are specific characteristics of the user’s EM environment that will not be covered by the usual EMC compliance tests. If so, develop a strategy for coping with them (design guides, additional tests, etc.) | [1] 1.2 |  |
| 1.3 | Check to see if the user(s) have specific installation characteristics that differ from what is good EMC practice and/or differ from what the team is used to. If so, develop a strategy for coping with them (design guides, additional tests, etc.) | [1] 1.2 |  |
| 1.4 | Define the EMC strategy that will be followed, for example:* Definition(s) of the RF Reference(s)
* Segregation between different functions
* Modularisation and/or number of PCBs
* Types of ICs
* Shielding (inc. how it will affect manufacturing, maintenance, servicing, etc.)
* Filtering
* PCB technology (e.g. THP, Microvia (HDI), etc.) and number of boards
* Internal interconnections for signals, data and power
* External interconnections for signals, data and power
 | [1] 1.2 |  |
| 1.5 | Assess whether the use of new technologies or design tools could reduce time-to-market or otherwise make the product more successful financially, e.g.:* X2Y devices
* Buried capacitance in the PCB (e.g. Faradflex)
* Blind and/or buried microvias (instead of THP)
* Feedthrough (3-terminal) capacitors
* Micro coax / twinax or fibre-optics for high-speed data cables
* Board-level shielding instead of module or overall product shielding
* Circuit simulations
* 2D field-solver simulations for PCBs, transmissions lines, etc.
* 3D field-solver simulations for structures, cables, enclosures, etc.
* Parameter extraction from field solvers into circuit simulator to ‘prove’ the SI, PI and EMC of the total design before first prototype made
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| 1.6 | Specify hardware, mechanical and interconnection requirements based on all of the above. | [1] 1.2 |  |
| 1.7 | Specify software requirements for enabling/disabling different parts/functions to help diagnose causes of emissions or susceptibility. | [1] 1.2 |  |
| 1.8 | Specify software requirements for creating the worst case conditions for emissions or immunity for each of the EMC tests that will be applied. | [1] 1.2 |  |
| 1.9 | Specify software requirements for the avoidance of all synchronous timing (where practicable) so that spread-spectrum clocks can be used for synchronous digital circuits, and possibly also for switched-mode power converters. | [1] 3.1.2, 3.4.4 |  |
| 1.10 | Specify software requirements that will deal with signal and data errors caused by intermittent connections, EMI, etc., in ways that maintain product operation with full or degraded functionality where appropriate.For example, momentary dimming of an indicator or hash on a display might not matter, when loss of indication or display would be unacceptable. | [1] 1.2 |  |
| 1.11 | Determine all areas where new technologies or new types of components will be used (even when competitors or other project teams have successfully used them) because they may have EMC characteristics that this project team has not previously encountered and has little/no expertise with. Examples include new device technologies, alternative types of microprocessor or memory, new types of display panels, new types of datalinks, new ways of manufacturing product enclosures, PCBs, etc.Develop strategies for de-risking any new design issues, for example: * Building and testing experimental boards to determine what SI, PI and EMC design techniques will be required to use them effectively, before designing them into the first prototype
* defining special test strategies
* at least making sure there is enough extra time and/or budget in project planning/cost, etc.
 | [1] 1.2 |  |
| 1.12 | Beware when reusing boards, schematics or software from previous projects.Ensure that their EMC performances are known and understood.Determine whether the EMC practices used in their design are appropriate for the new project. | [1] 1.2 |  |
| 1.13 | Perform "EMC design reviews" on the schematics, PCB layout, mechanics and software, prior to first prototype manufacture.Compare their EMC practices with this checklist to determine whether each item in this checklist was:1. Used in full
2. Used with modifications (document what and why)
3. Not used because not relevant (document why)
4. Not used because impractical (document why, and what was done instead to cover that EMC issue cost-effectively)
 | [1] 1.2 |  |
| 1.14 | Determine any influence of the test setup on the emissions and/or immunity and take appropriate steps where these do not reflect real-life operation. | [1] 1.2 |  |
| 1.15 | Perform EMC pre-compliance tests, document their results in detail, check whether any problems are found and develop a strategy for solving them. | [1] 1.4, 1.5 |  |
| 1.16 | Good emissions and immunity are essential for reliability, warranty returns rate, and customer satisfaction and low cost of future sales. So, perform highly accelerated life testing (HALT) and check EMC performance is maintained afterwards. Fix any problems that are revealed. | [1] 1.1 |  |
| 1.17 | Document the good EMC practices that were used for the various aspects of the product (schematic, component selection, PCB layout, mechanics, etc.) with any additional notes on why and how, where necessary, and store this with the project files so it can be referenced in future. | [1] 1.2 |  |
| 1.17 | Document all of the EMC-critical aspects of the design/construction (e.g. components, fixing methods, metal-finishes, etc.) with any additional notes on why and how, where necessary, and store this with the project files so it can be referenced in future, for example when approving a different supplier. | [1] 1.2 |  |

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| Circuit (schematic) design |
| *General Approach:* Design to keep *dV/dt* and *dI/dt* no larger than necessary at all times.  |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 2.1 | Take account of the influence on the emissions of the amplitudes, waveshapes and/or frequency ranges of the signals and data used in the product.Where necessary, minimise emissions by using lower frequencies in analogue circuits, slower raise/falltimes in switch-mode power and digital signals. Best is to use slower devices (e.g. quasi-resonant switch-mode controllers; program slower edge rates), next best is to make provision for simple filters on all output pins of digital devices.*Note:* It’s not just the signals that cause emissions. All devices that use digital processing suffer from ground-bounce and power-bounce noise that puts very broadband CM noise onto all of the device’s pins, even ones with static data or analogue outputs. However, the source impedance for CM noise emitted by input pins is about 4pF so these don’t (usually!) need filtering. | [1] 3.1.2, 3.2, 3.3, 3.4, 3.5 |  |
| 2.2 | Define the RF Reference (or References) to be used in all cases (usually PCB 0V planes, chassis, enclosure shields, etc.). | [1] 2.7.9, 2.7.10, 4.6.12, 7.4.1[2] 4 |  |
| 2.2 | Check whether all PCB traces and other interconnections (e.g. connectors, wires, cables) need designing as matched transmission lines. All outputs from digital devices made on sub-100nm silicon processes will probably need to be treated this way unless they can be filtered to significantly slow their edge rates. The degree of filtering (i.e. HF roll-off frequency) will depend on the electrical length (i.e. propagation time) of an interconnection (trace, connector pair, wire or cable). | [1] 3.5.2, 4.7, 7.8[2] 6Also see 4.11(cables) and 9.5 (PCBs) in this checklist |  |
| 2.3 | Employ (or make provision for) spread-spectrum clocking for every clock and power converter (where practicable). | [1] 3.1.2, 3.4.4 |  |
| 2.4 | Design all analogue circuits for good immunity.*Note:* If slew-rates exceed about 50V/microsecond, they may also need designing for low emissions. | [1] 3.2 |  |
| 2.5 | Where final design details are uncertain (e.g. how much signal filtering will be required), make provision for different options or topologies by dual-padding and the like on the PCB. But take care that the PCB placement for these options does not cause EMI problems due to stub lengths, floating long lines, etc. |  |  |
| 2.6 | Define all of the unused pins of an FPGA as high, low, or high impedance – don't let their status depend on the compiler. | [2] 8.8 |  |
| 2.7 | Define the treatment of all unused pins in connectors (and any unused conductors they connect to). Generally, they should be directly connected to the local RF Reference (e.g. PCB 0V or ground plane, chassis, shielded enclosure, etc.), but sometimes alternatives such as decoupled with capacitor to the RF Reference, pulled-up or pulled-down, resistively terminated in the characteristic impedance, etc., may be preferred. | [1] 4.4.1 |  |
| 2.8 | Ensure all unused components, such as amplifiers, logic gates, comparators, etc., are guaranteed to be in a well defined static state. Never let an input float, always connect them to the RF Reference or a power rail via a 1k resistor so that they can still be driven by board testers.  | [1] 3.1.2 |  |
| 2.9 | Apply all SI, PI and EMC design rules that are appropriate, and verify SI, PI and EMC performance, preferably by using validated simulation techniques, or (with much more cost and delay) by assembling and testing prototypes. | [1] 3 |  |

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| Component selection |
| *General Approach:* Choose parts that have good EMC performance, and keep *dV/dt* and *dI/dt* no larger than necessary at all times.  |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 3.1 | Choose ICs that measure as having lower emissions and/or higher immunity by close-field probe testing of supplier’s evaluation boards or own-made experimental boards.*Note 1:* Some ICs that provide similar functionality can have >40dB difference in EMC characteristics.*Note 2:* We hope that in the future, ICs data sheets will contain EMC emissions and immunity data. | [1] 3.1.1, 3.6 |  |
| 3.2 | Choose ICs (e.g. FPGAs) which allow output drive strength and rise/fall times to be programmed, so that they may be set to values that are no faster or stronger than necessary for reliable circuit operation. | [1] 3.1.1[2] 8.10 |  |
| 3.3 | Improve EMC whilst reducing overall cost of manufacture, by choosing devices with JTAG, and using this plus built-in self-test, functional tests, etc., to reduce the number of test pads for “bed-of-nails” testing of assembled boards, eliminating it completely if practicable.Also by using board assemblers who achieve better yields (even though they will cost more, the overall cost of manufacture should fall, and time-to-market should reduce).Where bed of nails testing is still required, use Hewlett-Packard’s “Bead Probe” techniques, because these probe beads cause fewer EMC problems than traditional probe pads.  | [2] 8.7 |  |
| 3.4 | Determine the maximum environmental specifications (peak voltage, peak current, peak power dissipation, clock speeds, maximum local ambient temperature, self-heating, etc.) that each component could possibly be exposed to over the anticipated lifetime of the product. Choose components (ICs, transistors, capacitors, inductors, ferrite beads, CM chokes, etc.) that have ratings that exceed the maximum.  | [1] 3.1.1, 3.3.1, 3.6, 3.8 |  |
| 3.5 | Define the incoming inspection regime for all EMC-critical components. E.g. sample-testing the surface conductivity of metal surfaces intended to be used for RF-bonding, quick-checking the emissions of a sample from each batch of purchased power supplies.(This will also help guard against assembling counterfeit components into products, with their very large associated risks.)  | [1] 3.7, 3.9 |  |
| 3.6 | When purchasing any subassemblies or modules, for example chassis-mounted power supply units or LCD panels, ensure that they comply with all of the safety and EMC standards that the product must comply with. EM emissions add up, so it might be important for the frequencies at which these subassemblies or modules have their maximum emissions to be different from those emitted by the rtest of the product, or else for their emissions to be at least 10dB below the limit the product has to meet. Take no-one’s word for any of this, or rely on any Declarations of Conformity or Test Certificates. Instead:1. Insist on receiving copies of the complete safety and EMC test results, from tests done by independent test laboratories accredited by their National Governments for each of the tests, for all of the required tests.
2. Carefully check through the test results to confirm that they are what you need, and that the tests were competently done and are relevant for how you intend to use the power supply.
3. Carefully check that the test results apply to the actual power supply unit you are thinking of purchasing for your product.
4. Check with the independent test laboratory that the test results you have been provided with are not faked.
5. Assess the manufacturer’s QA to check that it ensures that all manufactured power supplies comply with the same test results seen in ii) above. Such a QA process will include change controls that check every change proposal for its possible consequences for safety and EMC compliance; sample-based full testing for safety and EMC in serial manufacture plus basic safety tests on every unit manufactured; appropriate precautions against being supplied with counterfeit components.
6. Perform sample-based checks on all purchased power supplies to ensure that their EMC and Safety compliance is maintained, before accepting any power supplies into Manufacturing’s Stores.
7. Take all precautions against being supplied with counterfeit power supplies.

It is possible to shunt activities i) –v) onto Safety Agencies (such as TUV, UL, CSA, SEMKO, etc.) by purchasing only power supplies that they have approved and bear their Approval Marks. Some of these Agencies also operate similar approval schemes for EMC. When using Agency Approved power supplies, take no-one’s word for any approvals, or rely on any certificates provided by the supplier, instead:1. Insist on receiving copies of the complete Safety and/or EMC Agency Approval documents, covering all of the requirements
2. Carefully check through the Agency Approval documents to confirm that they are what you need, and that they contain no problematic “Conditions of Use”.
3. Carefully check that the Agency Approval documents apply to the actual power supply unit you are thinking of purchasing for your product.
4. Check with the Approval Agency that the Approval documents you have been provided with are not faked.
5. Perform sample-based checks on all purchased power supplies to ensure that their EMC and Safety compliance is maintained, before accepting any power supplies into Manufacturing’s Stores.
6. Take all precautions against being supplied with counterfeit power supplies.

*Note 1:* Buying low-cost mains power supplies and simply relying on suppliers’ declarations for their compliance is (literally!) a very dangerous business, as many electronic manufacturers have found to their great cost.*Note 2:* Your company is assumed to be a “professional integrator”, which means that any safety or EMC non-compliances resulting from the use of non-compliant subassemblies or modules is considered in law to be your company’s fault. After dealing with the legal issues resulting from such non-compliances, your company might consider suing their suppliers to recover their costs (and legal fees), but as the suppliers are probably based in a Far Eastern country there is little chance of success. | [1] 1.2, [2] 1.6, 1.7 |  |

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| **Unshielded interconnections** (wires, cables, flexi-PCBs, ‘stake’ connectors, etc.)*Note:* these practices apply equally to Shielded Interconnections, see below. |
| *General Approach:* Design so that DM and CM (i.e. stray) current loops have low impedance. This generally means routing DM and CM ‘return’ conductors very closely with their relevant ‘send’ conductors, for signals, data, control, power, etc. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 4.1 | Preferably use fibre-optic, free-space optical communications, or wireless communications instead of electrical conductors (because all conductors are “accidental antennas”). Note that wireless communications can cause EMI with their radio transmitters, and suffer EMI with their receivers. | [1] 4.2.2 |  |
| 4.3 | Position the connectors on each PCB so that their cables:* Can be fixed / bonded to the chassis as specified (see Section 4.7 in this checklist)
* Can be routed as efficiently as possible.
* Are as short as possible.
* Avoid crosstalk (i.e. near-field coupling) by routing far away from high-speed devices, switch-mode power converters, and any “Outside World” conductors that have not yet been suppressed.
 | [1] 4.3[2] 2.7 |  |
| 4.4 | Choose board-to-board connectors that provide a low impedance continuous ground plane connection, where practical.Alternatively, ensure that there are a large number of ground and power pins spread all over the length and breadth of the connectors. | [1] 4.4.2[2] 2.1 |  |
| 4.4 | Spread Power and Ground lines all over the length and width of all multiway connectors and cables, interleaving them with each other and with any signal or data lines. For example, when using a flat or round ribbon cable for example:* Interleave Power and Ground lines
* Interleave single-ended signal lines with one or more return lines (usually Ground)
* Differential pair lines must be interleaved to be as closely coupled together as possible, and sufficiently spaced from other lines to avoid significant crosstalk and/or unbalance.

Interleaved lines in cables are easiest to do by using twisted-wire-pairs, triples, quads, etc. Where interleaved wires pass through a connector, use adjacent connector pins that use the same pattern.Where a power/ground twisted pair cannot carry sufficient current, use two or more power/ground twisted pairs in parallel with each other. | [1] 4.4[2] 2.1 |  |
| 4.5 | Connect any/all unused conductors in any cable to the Ground (i.e. the RF Reference) at both ends of the cable. Except where they would cause problems for differential lines, add as many extra conductors that are grounded-at-both-ends as practical to every connector.Where direct connection to ground at both ends is not practicable, connect one end via a series capacitor rated for the maximum surge/transient overvoltage it will experience. Where none of the above is practical, remove the unused conductor from the cable. | [1] 4.4 |  |
| 4.6 | Ethernet™ connections:* Use connectors with integrated magnetics and CM filters. Where this is not possible, provide CM filtering on the board, as close as possible to the RJ45 connector.
* Choose shielded connectors with at least two contacts between each edge and the PCB 0V (= ground) plane, plus at least two contacts between each edge and the front/rear panel or chassis.
* Optimise mechanical design for optimal and reliable contacts with the front/rear panel or chassis.
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| 4.7 | Route all off-board cables close to a metal chassis all along their lengths.Avoid routing wires or cables across any joints or seams between different metal areas, or across any apertures in a metal area.Where this is impractical, provide a wide conductive bridge (e.g. metal tape) under, or a cylindrical shield around the wire or cable, RF-bonded to the metal areas on each side of the joint, seam or aperture. (This provides a continuous nearby path for the stray Antenna Mode (i.e. CM) currents that leak from the wire or cable, thereby reducing accidental antenna degradations of emissions and immunity.)  | [1] 4.4 |  |
| 4.8 | Specify the position, routing, and enough mechanical fixings of all off-board cables along their entire length. Don’t leave this to the assembly person. |  |  |
| 4.9 | Ensure that all wires and cables that exit or enter the product’s enclosure are reliably fixed in specified routes that take them as far away as possible from all internal wiring/cabling and PCBs.Where this is not practicable, use cable and PCB shielding to prevent crosstalk and/or near-field coupling that could arise. | [1] 4.3 |  |
| 4.10 | Make provision for fitting CM chokes (ferrite cores) to each cable itself, to dampen the resonant frequencies that cause excellent (but unwanted) “accidental antenna” behaviour, including providing enough space, mechanical fixations, etc.Cable resonant frequencies depend on their length, routing and electrical terminations, and may be simulated by a field solver, measured on an experimental set-up, or measured on a prototype (in descending order of ability to reduce time-to-market and increase profitability).Ferrite cores should be a close fit to the cables’ outside diameters.Ferrite cores have very high relative permittivity, so mounting them on the RF Reference (usually the chassis or enclosure) adds CM capacitance and increases the suppression they provide. | [1] 5.2.6 |  |
| 4.11 | Use matched transmission line cables and connectors, where appropriate. | [1] 4.7 |  |
| 4.12 | Specify the physical characteristics of every cable assembly, for all (potential) cable manufacturers (including second and third sources).* All parts must be defined (Manufacturer, type)
* Datasheets of all the assembled parts must be available
* All relevant specifications must be verified and validated
* Electrical parameters and their tolerances must defined
	+ Characteristic impedance (Single-ended or Differential)
	+ Number of twists/length
	+ Which wires must be paired/twisted
	+ How must the shields be connected

In addition, it might be necessary to specify their SI and/or EMC characteristics. | [1] 3.9 |  |

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| **Shielded interconnections**(wires, cables, flexi-PCBs, etc.)Note: the good EMC practices for unshielded interconnections, above, also apply to shielded types. |
| *General Approach:* Treat cable shielding like water or gas plumbing – i.e. gaps means leaks. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 5.1 | Determine the quality of a cable’s shield and its shielded connectors (i.e. their Shielding Effectiveness: SE) by comparing the frequencies and their levels of the DM (wanted) and CM (unwanted noise) signals or power in that cable with the emissions/immunity specifications to be complied with, taking into account the accidental antenna characteristics of the inner conductors (that are to be shielded).However, the CM noise’s frequencies and their levels are often unknown until simulated by a 3D field solver, or tested on an experimental board, or tested on a prototype (in descending order of preference for the lowest time-to-market). | [1] 4.6 |  |
| 5.2 | Determine whether shielded cables inside a shielded product enclosure can have their SE requirements reduced by the SE of the enclosure. Note that both of these vary with frequency. |  |  |
| 5.3 | Shielded connectors should generally achieve reliable 360° metal-to-metal electrical bonding between the cable’s shield and its connector body, and also between its connector body and the item being connected to (either another connector body, or a product’s metal chassis).Where connectors are not used, 360° shield-bonding cable glands are best, but saddle-clamp or even P-clip shield bonds may be acceptable where SE requirements are not very high.RF-bond all cable shields at both ends, to the local RF Reference (usually the local chassis). (Single-ended shield bonding just creates efficient ‘accidental antennas’, and always has been a bad practice for EMC despite its widespread use.)It is not recommended to use a drain wire, twisted braid, or soldered wire (usually known as ‘pigtails’) or connector pins, to RF-bond the shield of a shielded cable to the body of a connector or a chassis, however this can be acceptable where SE requirements and the frequencies to be shielded are low.(Beware, if there is a digital processor or switch-mode converter in the product, even “static” or low-frequency signal lines will be ‘polluted’ with CM noise at RF frequencies, even up to several GHz.) | [1] 4.6.5, 4.6.6, 4.6.7, 4.6.12 |  |

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| Filtering |
| *General Approach:* Design impedance discontinuities that reflect the unwanted propagating conducted EM waves (i.e. noises) or convert them into heat. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 6.1 | Determine the three-dimensional physical boundary(ies) between all of the “Inside-World(s)” and the “Outside-World”. This is sometimes called “circuit segregation”, or simply “segregation”. | [1] 5.1, 6.1, 7.2[2] 2.1, 2.6 |  |
| 6.2 | Make provision for filtering (and surge/transient/ESD protection) at each and every point where a conductor (whether it carries power, signal, control, data, earth/ground, or is non-electrical) crosses the boundary(ies) between the “Inside-World(s)” and the “Outside-World”. | [1] 5.3.3, 6.3.16, 6.4.10[2] 2.1.6, 2.6 |  |
| 6.3 | Where there are nested “Inside Worlds” (also called EM Zones) determine the three-dimensional physical boundary(ies) between them. This is sometimes called “circuit segregation”, or simply “segregation”, and always applies (for example) at board-board connectors. | [1] 5.1, 6.1, 7.2[2] 2.1, 2.6 |  |
| 6.4 | Where there are nested “Inside Worlds” (i.e. one inside the other) make provision for appropriate filtering at each and every point where each conductor (whether it carries power, signal, control, data, earth/ground, or is non-electrical) crosses a boundary between “Inside-Worlds”. | [1] 5.3.3, 6.3.16, 6.4.10[2] 2.1.6, 2.6 |  |
| 6.5 | Synergy of filtering and shielding. Where PCB or enclosure shielding is used for any “Inside Worlds”, the effectiveness of each filter (in dB attenuation/frequency) on each conductor that crosses a boundary between “Inside-Worlds” – or between any “Inside-World” and the “Outside-World” – should correspond with the shielding effectiveness of the relevant shield, over the frequency range to be controlled.  | [1] 5.3.3, 6.3.16, 6.4.10[2] 2.1.6, 2.3, 2.6 |  |
| 6.6 |  All conductors (whether carrying power, signal, control, data, earth/ground, or non-electrical) entering or exiting a shielded volume, or an area of RF Reference plane on a PCB (= 0V plane, ground plane), must at least have a capacitor filter shunt-connected to the shield wall or PCB’s RF Reference plane at the point of entering or exiting, to provide local return paths for CM currents on the conductors. If a conductor can be directly bonded to the shield wall or PCB’s RF Reference plane at the point of entering or exiting, this should be done instead of using a filter. | [1] 5.3, 6.3.16, 6.4.10[2] 2.1.6, 2.6 |  |
| 6.7 | Where practical, determine the source impedances of the DM and/or CM noises to be filtered, and the DM and CM impedances of the load, and design the filter accordingly to optimise the attenuation over the frequency range to be controlled.Where these impedances are not known, use at least one stage of filtering using a Tee or  design. Tee designs are recommended for general use. | [1] 5.2 |  |
| 6.8 | Make provision for CM chokes in all filters for power and signals, data, control, etc. EMC testing might discover that CM chokes can be replaced by individual ferrite beads or even zero-ohm links. | [1] 5.2[2] 2.6 |  |
| 6.9 | All DC/DC converters should be fitted with series-ferrite filter beads (having adequate current capacity given the maximum local ambient temperature), directly at their inputs and outputs. This assumes that the input and output power rails that connect to the DC/DC converter are fitted with decoupling capacitors that are effective up to 1000 times the DC/DC converter’s switching rate. If necessary, add more decoupling capacitors (or embedded PCB capacitance) to achieve this. |  |  |
| 6.10 | Ideally, circuit segregation should result in each different power rail occupying a single area on a PCB.Where the same power rail has to connect to different locations far-apart on the board, it is generally best to create areas of power plane (sometimes called “islands”) that are as small as practical in each location, interconnecting them via Pi filters, also see Section 9.4 in this checklist. | [2] 5.3.8 |  |
| 6.11 | Filter RF and safety bonding methods (e.g. screws, rivets, conductive epoxy, solder, wires, conductive gaskets, etc.) must be reliably low-resistance over the anticipated lifetime of the product, taking into account shocks and vibrations, oxidation of metal surfaces, galvanic corrosion, temperature fluctuations causing movement due to different temperature coefficients, etc. Ensure that the DC resistance of each filter ground bond will reliably be less than 10 milliohms (ideally < 1milliohms) over the anticipated lifetime of the product.Ensure that the RF impedance of each filter ground bond will reliably be less than 1 ohm (ideally < 100milliohms) at the highest frequency to be controlled over the anticipated lifetime of the product.It is recommended to sample-check these in production as part of the QA process. | [1] 5.3, 6.6, 6.7 |  |
| 6.12 |  Where coils, chokes and other inductors associated with different circuits are closer together than their sizes, they should generally be oriented at 90° to each other to minimise their magnetic field coupling.However, individual ferrites or inductors in series with the send and return paths of a given power, signal, data, control, etc. interconnection in place of a CM choke – these should be placed side-by-side and in the same orientation to get the best filtering effectiveness. |  |  |
| Transient/Surge suppression |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 7.1 | Galvanic isolation is generally a better & more reliable design solution than transient/surge suppression.  | [1] 5.5.4 |  |
| 7.2 | Filters can be used to suppress transients and surges. Resistor-capacitor filters are best for this, but inductor/choke-capacitor filters can be acceptable if their natural resonances are controlled well enough.  | [1] 5.5.5 |  |
| 7.3 | Design any transient/surge protection to ensure that overvoltages and overcurrents on cables that enter/exit the product do not damage any part of the product.  | [1] 5.5 |  |
| 7.4 | Design any transient and surge protection used on signal, control, data lines so that it does not have so much capacitance that it degrades signal integrity.  | [1] 5.5.16 |  |
| 7.5 | Design any transient and surge protection so that short-circuit failure of any devices cannot cause a safety hazard, e.g. by coordinating mains suppressors with mains fusing.  | [1] 5.5.13 |  |
| 7.6 | The locations of transient/surge protection components for protecting the “Inside-World” from the “Outside-World” are determined by the same techniques as for filters. | Use 6.1 and 6.2 in this checklist |  |
| 7.7 | Where transient/surge protection is required between different parts inside a product, the locations for the components are determined by the same techniques as for filters. | Use 6.3 and 6.4 in this checklist |  |
| 7.8 | Protect against systematic transients and surges (e.g. earth-lift or ground lift voltages) | [1] 5.5.19 |  |
| 7.9 | Ensure that data cannot be corrupted by transients and surges (even when devices are not damaged) | [1] 5.5.20 |  |
| 7.10 | Suppression components, and conductors (traces, wires, etc.) that carry transient/surge voltages/currents, must be adequately rated for their worst-case repetitive peak voltages, peak currents, peak powers, and peak temperatures (having regard to the worst-case local ambients) over the anticipated lifetime of the product.However, where regular maintenance is required, it can be practical to use less-rugged suppressors providing it is made easy and practical to check the status of transient/surge suppressors and replace them if they are showing signs of wearing out. The typical wear-out period should be at least three times the maintenance period, more if the consequences of failure are more severe.  | [1] 5.5.1, 5.5.2, 5.5.10-14 |  |
| 7.11 | Suppression component EMC and safety bonding methods (e.g. screws, rivets, conductive epoxy, solder, wires, conductive gaskets, etc.) must be reliably low-resistance over the anticipated lifetime of the product, taking into account shocks and vibrations, oxidation of metal surfaces, galvanic corrosion, temperature fluctuations causing movement due to different temperature coefficients, etc.  | [1] 5.3, 6.6, 6.7 |  |

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| Shielding(i.e. of enclosures, PCBs, etc., see section 5 for shielding interconnections) |
| *General Approach:* Design impedance discontinuities that reflect the unwanted propagating radiated EM waves (i.e. noises) or convert them into heat. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 8.1 | Shield with metal planes.Providing an RF Reference plane (e.g. a metal sheet, PCB 0V plane, etc.) that is very close indeed to all of the components and conductors (cables, PCB traces, etc.), plus using only low-profile components, provides a degree of shielding that may be sufficient in itself, or at least reduce the specification and hence cost of any volumetric shields that are used. | [1] 6.2 |  |
| 8.2 | Use shielded volumes. PCB-level shielding is generally recommended as having lower overall-cost-of-manufacture than using an overall shielded enclosure.  | [1] 6.3.1, 6.4.1[2] 2.2 |  |
| 8.3 | Determine the three-dimensional physical boundary(ies) between all of the “Inside-World(s)” and the “Outside-World”. This is sometimes called “circuit segregation”, or simply “segregation” or “EM-zoning”, and tells us where to place any shielding barriers.  | [1] 5.1, 6.1, the intro to 6.3 on page 243, 7.2[2] 2.1, 2.6Also see Section 6.1. |  |
| 8.4 | Make provision for shielding at each and every “Inside-World(s)” and the “Outside-World” boundary.  | [1] 5.1, 6.1, the intro to 6.3 on page 243, 7.2[2] 2.1, 2.6Also see Section 6.2. |  |
| 8.5 | Where there are nested “Inside Worlds” (also called EM Zones), determine the three-dimensional physical boundary(ies) between them. This is sometimes called “circuit segregation”, or simply “segregation” or “EM-zoning”, and always applies (for example) at board-board connectors. It tells us where to place any internal shielding barriers. | [1] 5.1, 6.1, the intro to 6.3 on page 243, 7.2[2] 2.1, 2.6Also see Section 6.3. |  |
| 8.6 | Where there are nested “Inside Worlds” (i.e. one inside the other) make provision for appropriate shielding barriers at the boundaries between them. | [1] 6.3.1Also see Section 6.4. |  |
| 8.7 | Synergy of filtering and shielding. | See Section 6.5. |  |
| 8.8 | Design the shielding effectiveness for each shielded volume, taking into account:* The emissions/susceptibility of the product’s hardware and software, the emissions/immunity standards to be complied with, and the real-life electromagnetic environment of the users (which may require going beyond complying with the standards to have a product with acceptable (or lower) warranty costs).
* Whether near-field and/or far-field shielding are required, the level of shielding effectiveness required in each case, and how it varies with frequency.
* Skin depth (varies with frequency and type of metal)
* The dimensions and shapes of the shielded volumes and resulting cavity resonances (ideally use small shielded volumes that have their lowest resonant frequencies higher than the highest frequency to be controlled, e.g. by using PCB-level shielding).
* Degradations caused by gaps and apertures at seams, joints, ventilation, etc.
* Degradations caused by surface conductivity of the metal or metallised parts used to construct the shields and how they can degrade over time due to oxidation (note that plain aluminium oxidises over time and loses its surface conductivity), galvanic corrosion, fretting corrosion, cracking corrosion, wear, loosening of fixings due to vibration, temperature cycling, etc., all depending on users’ environmental parameters.
* Degradations caused by conductive gaskets.
* Degradations caused by the impedances of the fixings used to assemble the shielded volume (seam-welding gives the best results)

Ensure that the DC resistance of each shield connection or joint will reliably be less than 10 milliohms (ideally < 1milliohms) over the anticipated lifetime of the product.Ensure that the RF impedance of each of each shield connection or joint , will reliably be less than 1 ohm (ideally < 100milliohms) at the highest frequency to be controlled over the anticipated lifetime of the product.It is recommended to sample-check these in production as part of the QA process. | [1] 6.3, 6.4, 6.5, 6.6, 6.7, 7.3[2] 2.2 |  |
| 8.9 | Ensure that insulating surfaces and contacts are not insulated or made high-resistance by the use of chemical thread-lock compounds, polymer passivating films, etc., and devise simple, quick, low-cost checks for use at Goods-In to prevent batches of shielding parts that have had such materials applied from being accepted.  | [1] 6.7 |  |
| 8.10 |  LCD panels, panel meters, and similar parts may be used as parts of shielding enclosures, in which case they must either be supplied with a low surface-resistance metal rear cover made as a single metal part (e.g. a stamping), or supplied with a shielded window with a low surface-resistance surround, either of which can be assembled into the shielded volume concerned. Alternatively, where neither a rear cover nor shielded window is supplied with the unit, one or the other must be provided by the assembly of the product.Overall design of the shielded volume comprising the LCD panel, panel meter, etc., must follow Section 8.9 in this checklist. | [1] 6.3.12Also apply section 8.9 in this checklist. |  |
| 8.11 |  Reliable, low surface-resistance, corrosion-protected areas must be provided wherever shielded connectors, cable shields or metal-bodied filters are to be assembled to a chassis, shielded area or shielded volume (even if on a PCB). | [1] 4.6.5, 4.6.7, 4.6.12, 5.3, 6.3.16, 6.4.9, 6.7 |  |

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| Printed Circuit Boards (PCBs) *without* high-speed data busses or comm’s |
| Circuit segregation within PCBs |
| *General Approach:* Segregate areas of circuitry with different functionality, over a single RF Reference plane (e.g. 0V/ground plane) that extends beyond them all. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 9.1.1 | Where practicable, use a single PCB rather than two or more boards with interconnections. This will be more reliable, and will:* Reduce BOM cost by reducing costs of connectors, cables and EMI mitigation measures (shielding, filtering , transient/ESD suppression, etc.)
* Reduce overall cost of manufacture (including the costs of fixing faults and warranty returns)
* Create simpler resonant structures that are easier to deal with for EMC emissions and immunity.

However, “flexi-rigid” construction using a single RF Reference on a dedicated board layer for the entire structure behaves like a single PCB and is acceptable. All the usual design rules for RF References must be observed (see Section 9.3 of this checklist).*Note:* A three or four layer flexi with the outer layers devoted to RF Reference planes and stitched together with vias along both edges can be used to replace shielded cable interconnections. See Section 5 of this checklist. | [1] 7.2[2] 2.1 |  |
| 9.1.2 | The circuits on the board must be physically partitioned (= segregated, zoned) so that sensitive parts/circuits occupy a different area of the board than from noisy parts/circuits.No traces, wires or components can be located or extended outside of their segregated area (except the RF Reference, see Note 1 below) except where they must interconnect between two or more segregated circuit areas (see Note 2 below). *Note 1:* The RF Reference (usually the 0V or Ground plane) must be continuous across the entire board area, including all of the segregated circuit areas, because return currents have to flow between the various segregated circuit areas and this provides the optimum paths for them. See Section 9.3 in this checklist.*Note 2:* All of the interconnections between segregated areas might need to be fitted with filtering, shielding or surge suppressors, see Section 9.2 in this checklist.  | [1] 7.2[2] 2.1 |  |
| 9.1.3 | Locate all PCB-cable connectors along one edge, ideally near to one corner, of each PCB. Don’t sprinkle them all over the board! | [1] 7.2[2] 2.7 |  |
| Interface analysis and suppression on PCBs |
| *General Approach:* Suppress interfaces between areas of circuitry on the PCB, and between the PCB and other PCBs or the Outside World. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 9.2.1 | Analyse each essential interconnection between segregated areas (see Section 9.1 in this checklist) for CM and DM noises that could be generated within each area, or that each area could be especially susceptible to.Then make provision for effectively attenuating any significant noises with filters and/or transient/surge suppressors located at the boundaries of the relevant segregated areas. SI and EMC testing will discover whether the filters and/or transient/surge suppressors are needed, and what their design should be. *Note:* Sections 6 and 7 of this checklist cover filtering and transient/surge suppression techniques. | [1] 7.2, 7.3[2] 2.1, 2.6 |  |
| 9.2.2 | Make provision for shielding individual ICs or segregated circuit areas on each PCB; whole PCBs; complete sub-assemblies or modules, complete products, in that order.*Note 1:* shielding at the lowest level of assembly (i.e. individual ICs or segregated circuit areas) costs least in components and assembly time, and suffers least from cavity resonances occurring within the frequency range to be controlled.*Note 2:* Sub-assembly, module and overall enclosure shielding is covered by Section 8 in this checklist, but the same general rules for designing shielding apply to board-mounted shields. | [1] 7.3[2] 2 |  |
| 9.2.3 | Do not route any traces or power planes near to or underneath board-board or board-cable connectors, on any layers, even if it appears that they are ‘shielded’ by ground planes. | [1] 7.2, 7.3[2] 2.1, 2.6 |  |
| Reference / Return / 0V (i.e. “Ground”) and Power planes on PCBs |
| *General Approach:* Segregate areas of circuitry with different functionality, over a single RF Reference plane (e.g. 0V/ground plane) that extends beyond them all. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 9.3.1 | Identify the RF Reference for each PCB (or flexi-rigid PCB assembly as described in Section 9.1.1 if this checklist) and provide at least one dedicated copper layer for it over the maximum copper area possible.This will usually be what is usually called the 0V plane or Ground plane.*Note:* Split planes create RF resonances, and anyway are not very effective above 100MHz and ineffective above 1GHz, so should no longer be used. The potential problems caused by the circulating currents from other circuit areas are dealt with much more effectively than is possible by splitting planes by some of the other PCB techniques covered in Section 9 of this checklist. These days, the only reason for splitting a RF Reference is where galvanic isolation is necessary, see Section 9.3.2 in this checklist. | [1] 7.4.1, 7.4.2, 7.4.3, 7.4.4, 7.4.7[2] 4.1, 4.2 |  |
| 9.3.2 | Planes used for ‘shielding’ or ‘chassis’ inside a PCB stack-up, and not carrying any circuit currents, are RF resonators and no longer effective, so must not be used. | [1] 1.4 |  |
| 9.3.3 | Where any RF Reference plane (see Section 9.3.1 in this checklist) is split (e.g. for galvanic isolation at DC or powerline frequencies) the split must be RF-bonded with capacitors spaced all along the split.But where the split is required to provide galvanic isolation at RF and RF-bonding cannot be used, shielded optical, wireless, or magnetic (i.e. transformers) should be used to pass power, signals or data across the split, so that there are no return currents that need to cross the split.  | [1] 7.4.5, 7.4.6[2] 4.3, 4.4 |  |
| 9.3.4 | It may prove beneficial to remove plane areas (and all traces not associated with the circuit) from under filtered unshielded connectors, to reduce the stray capacitance shunting across series filter elements.  | [1] 7.3[2] 2.6.4 |  |
| 9.3.5 | Power should generally be provided by power planes that create a distributed decoupling capacitance to an adjacent RF Reference plane.Decoupling is covered in Section 9.4 of this checklist. | [1] 7.4.1, 7.5.3, 7.5.4[2] 5.3 |  |
| 9.3.6 | Where traces must cross splits in the plane(s) that carry their return currents, make provision for the return currents to cross the splits, ideally with CM chokes but other methods are possible, depending on the frequency ranges associated with the traces. | [1] 7.4.5[2] 4.2.12, 4.4, 6.3.4, 6.3.5, 6.3.7, 6.4.3 |  |
| 9.3.7 | No components, traces or power planes must be located or routed closer than 3mm to the perimeter of the RF Reference plane, except for the perimeter guard trace (Section 9.3.8 in this checklist). Larger spacings than 3mm are better for EMC, and it can be cost-effective to make boards larger just to accommodate larger RF Reference plane areas.  | [1] 7.4.1[2] 4.2.1 |  |
| 9.3.8 | Where there are parallel 0V or power planes having the same voltage on different PCB layers, they must be bonded together with via holes on a 10mm (or smaller) grid to help prevent cavity resonances from occurring within the frequency range to be controlled. | [1] 7.5.4[2] 4.2.8, 4.2.9, 4.2.11 |  |
| 9.3.9 | Provide a perimeter guard trace on every layer other than those used for the RF Reference, aligned with the edge of the RF Reference plane(s) and bonded directly to it (them) by closely-spaced vias or edge-plating all around the perimeter.The guard trace should be no narrower than 2.8mm (to fit within a 3mm ‘no component, trace or power plane’ border described in Section 9.3.7 of this checklist). Just as Section 9.3.7, a wider guard trace is better for EMC, and it can be cost-effective to make the board larger to accommodate this.  | [2] 4.2.10 |  |
| 9.3.10 | Connect the RF Reference to the chassis (which could be an external metal enclosure) at multiple points regularly spread all over the area of every board, either using direct connections or RF-bonds with series capacitors. The chassis bond spacing governs the highest frequency that this technique is effective up to, so choose an appropriate spacing.*Note:* Where a plain plastic enclosure is to be used with no metal chassis, make provision for these chassis bonds anyway, because using them in conjunction with a low-cost sheet of metallised plastic or cardboard, or thin metal, used as the chassis may help solve many EMC problems. | [1] 7.4.4[2] 3 |  |
| 9.3.11 | Ensure there is a bond between the RF Reference and the chassis or metal enclosure located very closely to each cable connected to a board.This bond must have a low impedance (i.e. < 1 ohm) at the highest frequency to be controlled.Where the cable is more than 10mm wide (e.g. a ribbon cable) there should be one such bond every 30mm or less along the length of the connector. A conductive gasket bond that is as long as the connector would be ideal. |  |  |
| 9.3.12 | Ensure that the DC resistance of each connection to the RF Reference, and of each direct chassis bond will reliably be less than 10 milliohms (ideally < 1milliohms) over the anticipated lifetime of the product.Ensure that the RF impedance of each connection to the RF Reference, and of each RF-bond to the chassis, will reliably be less than 1 ohm (ideally < 100milliohms) at the highest frequency to be controlled over the anticipated lifetime of the product.It is recommended to sample-check these in production as part of the QA process. |  |  |
| 9.3.13 | It is impossible to have solid 0V or power planes under BGA devices, without using microvia PCB manufacturing techniques, and this should be considered because of the EMC benefits.So, when using THP, it is very important for EMC to achieve a complete mesh under all BGAs, for any/all planes. This means using appropriate track-and-gap width rules in the layout.*Note:* Microvia boards, and THP boards with track-and-gap of 4 thousands of an inch (100 microns) are now available from many Far Eastern PCB suppliers without a price premium.  | [1] 7.4.2 |  |
| Power rail decoupling on PCBs |
| *General Approach:* Provide low-impedance power rails for each segregated circuit area, so their circulating power currents remain local. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 9.4.1 | Every component that can source, or can be upset by, power rail RF noise must have at least one multilayer ceramic decoupling capacitor of 10nF or more connected to its power supply as close as practical to the component with very low-impedance connections to its power rail and local RF Reference Plane.*Note:* decoupling for SI may add additional requirements at lower frequencies, for example the total amount of bulk decoupling, which is not covered in this checklist. | [1] 7.5[2] 5.1, 5.2 |  |
| 9.4.2 | Decoupling should maintain a low impedance for each DC power rail over the entire frequency range for which EMC problems could occur. This will generally require many different values of multilayer ceramic capacitors spread all over each power plane area, spaced no more than 25mm apart to reduce the high-impedance peaks caused by parallel resonances (sometimes called antiresonances).It will also require very low inductances in all decoupling capacitor board layouts, because above about 300MHz this inductance is the determining factor in achieving effective low-impedance decoupling. | [1] 7.5[2] 5.1, 5.2 |  |
| 9.4.3 | Parallel 0V and power planes on closely-spaced adjacent layers are generally required for all types of circuits, to provide a distributed decoupling capacitance with low impedance above 300MHz.Layer spacing should be less than 10 thousands of an inch (250 microns), ideally 2 thousands of an inch (50 microns) or less. | [1] 7.5.3[2] 5.3 |  |
| 9.4.4 | Special closely-spaced-layer PCB substrate materials are available (e.g. from Faradflex) for use in PCB manufacture, which can provide more than 1nF per square centimetre with highly-damped cavity resonances. It can be practical and cost-effective to use these PCB materials to achieve RF decoupling instead of large numbers of MLC capacitors. | [2] 5.3.15 |  |
| 9.4.5 | Power plane islands.Where the same power rail has to connect to different locations far-apart on the board, it is generally best to create areas of power plane (“islands”) that are as small as practical in each location, interconnecting them via Pi filters.Another reason for dividing a power plane into islands connected by Pi filters is to help prevent the noises from an especially noisy component or circuit area (e.g. a clock buffer) from circulating widely in that power rail. | [2] 5.3.7 |  |
| Transmission Lines and other trace routing issues on PCBs |
| *General Approach:* Route traces to avoid impedance discontinuities that cause them to resonate and behave as accidental antennas. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 9.5.1 | General routing rules for all traces on all layers:1. Firstly route all decouplers (low-inductance routing ensures they don’t restrict other traces)
2. Secondly route the signals with the fastest digital edges (typically: clocks; write strobes on SRAMs and FIFOs; output enables and chip enables; high-speed serial data) on a single board layer (i.e. no via holes along their lengths) ideally next to the 0V layer of a 0V/power plane pair, ideally using striplines with via holes at each end (but not along their lengths), keeping them far away from any plane edges or splits, and using 45° angles or curves instead of 90° corners.
3. Very sensitive signals can be routed as for ii) to improve their immunity
4. Thirdly, route any parallel data busses
5. Finally, fit all the other traces in
 | [1] 7.6.6[2] 6.3.1 |  |
| 9.5.2 | Outer layers should be reserved for surface-mounted or leaded components and their (short) connections to traces routed on inner layers. All free space on outer layers should be dedicated to filled-in areas connected to the dedicated RF Reference plane(s) by bonds spaced no more than /15 apart at the highest frequency to be controlled. |  |  |
| 9.5.3 |  Trace length (delay) compensation should use gentle serpentines, not sharp bends. | [2] 6.3.6 |  |
| 9.5.4 | Analyse the edge rates (or maximum frequencies) in every trace, considering both the DM (wanted) signals/data and the (unwanted) CM noises on it. If working in the time domain, ensure that the minimum risetimes are never more than one-third of the propagation delay of each trace (ideally, never more than 1/8th) .Alternatively, working in the frequency domain, ensure that the wavelength of the highest frequency to be controlled is longer than seven times the overall trace length (ideally longer than 30 times), remembering that the wavelength of traces in/on a glassfibre PCB are roughly half as long as wavelengths in air.)Where traces cannot meet the above requirements, either filter them at the source of their signals/data to achieve them, or use the matched controlled-impedance transmission line techniques described below. | [1] 7.6.1[2] 6.1, 6.1.6 |  |
| 9.5.5 | For each controlled-impedance transmission-line trace (or trace pair) select the most suitable trace/plane geometry and layer stack that achieves the desired impedance without causing problems for routing (e.g. traces too wide) or manufacture (traces too narrow). | [1] 7.6.1[2] 6.1, 6.4.2 |  |
| 9.5.6 | Controlled-impedance traces must maintain the desired impedance over every segment of a trace having a propagation delay no more than 1/10th of the minimum risetime (equivalent to a length of 1/40th of the wavelength at the highest frequency to be controlled.The capacitive loading of component pins/pads, and stub or branch traces having propagation delays less than 1/20th of the minimum risetime, must be taken into account. In the case of differential traces, maintain the same spacing between them along their entire lengths, and place any via holes at the same locations along each trace in the pair, to control both DM and CM modes of propagation in every trace segment. | [1] 7.6.2, 7.6.6[2] 6.1.13 |  |
| 9.5.7 | Stub or branch traces having propagation delays longer than 1/20th of the minimum risetime, must be actively buffered, otherwise it will be impossibly to maintain good SI and EMC for them.  | [1] 7.6.7[2] 6.3.3 |  |
| 9.5.8 | To help avoid mismatches in characteristic impedance, ensure there is always at least 5W spacing between the trace concerned (width W) and all other traces and areas of copper on the same layer.Alternatively, take the proximity to traces and copper areas into account in the design of the trace.In any case, do not permit PCB manufacturers to modify any copper layers for reasons of copper balancing – the layers must be designed to achieve the required characteristic impedance for each controlled-impedance trace with the desired copper balancing taken into account. | [2] 7.4, 8.14 |  |
| 9.5.9 | All controlled-impedance traces must be terminated in a matching resistance having the same value at one end (ideally at both ends). Differential (balanced) traces should match both the CM and DM modes of propagation along their trace-pairs. | [1] 7.6.4[2] 6.2, 6.4.2 |  |
| 9.5.10 | Ensure the length of each trace in a differential (balanced) pair is the same, taking all connectors and cables into account, with a maximum tolerance that ensures the difference in propagation delays between the two traces is less than 1/10th of the risetime (equivalent to 1/40th of the wavelength at the highest frequency to be controlled).Any trace length matching must not result in variations in the spacing between the two traces. | [1] 7.6.2[2] 6.4.4 |  |
| 9.5.11 | Where the return paths for traces must change layers, the layers must be RF-bonded using at least to vias or capacitors arranged symmetrically either side of the trace.This is especially a problem for traces routed on layers adjacent to power plane layers, because power plane layers are often split to provide different voltage rails.  | [1] 7.4.5, 7.4.5[2] 4.2.12, 4.4, 6.3.4, 6.3.5, 6.3.7, 6.4.3 |  |
| Stack-ups, micro-vias (HDI), and miscellaneous issues for PCBs |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 9.6.1 | The number of layers, and the way they are stacked up, must be at least the minimum required to:1. Prevent harmful interactions between power layers and signal-layers
2. Prevent harmful crosstalk between signals on adjacent signal layers
3. Provide distributed decoupling capacitance for each power plane (Sections 9.3.3. and 9.4.4)

*Note 1:* Not using the number of board layers required for good EMC design almost always adds more cost overall than the saving in the cost of the bare board. Also, it delays time-to-market, which has been more important for profitability than BOM cost since 2000.*Note 2:* Different PCB manufacturers specialise in specific numbers of layers, although they usually don’t make this clear. So to add layers without incurring significantly higher bare-board costs it is often necessary to go to different suppliers from those currently used. | [1] 7.7[2] 7.2 |  |
| 9.6.2 | There should be a dedicated RF Reference plane on the next layer in from any component side.Where one side of the PCB has no components mounted on it, it should be a dedicated RF Reference plane. | [1] 7.4.1, 7.5.3, 7.5.4[2] 5.3 |  |
| 9.6.3 | Where the number of layers exceeds eight, consider using microvia PCB construction to reduce the bare board cost.*Note:* If the quotations for bare-board cost when using microvia construction are significantly higher than for through-hole-plate (THP), this means that certain microvia suppliers have not been contacted. | [2] 7.5 |  |

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|  Electrostatic Discharge (ESD) suppression |
| *General Approach:* Either stop direct discharges from happening by insulating, or else use shielding and suppression designed for 3GHz or more.Usually both are needed. |
|  | **Good EM Engineering Practice** | **References** | **How applied** |
| 10.1 | All components must be adequately protected against foreseeable ESD by using galvanic isolation (plastic enclosures, knobs, etc.) and/or shielding (see Section 8 of this checklist).Even where plain plastic housings provide perfect protection against direct ESD events, shielding might still be needed to protect from the intense electrical and magnetic fields caused by nearby indirect ESD events. | [1] 8.2, 8.3, 8.4, 8.8, 8.9 |  |
| 10.2 | All I/O connector pins must be adequately protected against foreseeable ESD by suppression components that shunt the ESD transients directly to the RF Reference using very low-inductance connections. | [1] 8.5 |  |
| 10.3 | The locations of ESD suppression components for protecting the “Inside-World” from the “Outside-World” are determined by the same techniques as for filters. | Use 6.1 and 6.2 in this checklist |  |
| 10.4 | Protect against systematic ESD transients (e.g. earth-lift or ground lift voltages caused by ESD) | [1] 8.6 |  |
| 10.5 | Ensure that data cannot be corrupted by ESD transients (even when no devices are damaged) | [1] 8.7, 8.8, 8.9 |  |
| 10.6 | ESD suppression components must be adequately rated for their worst-case repetitive peak voltages, peak currents, peak powers, and peak temperatures (having regard to the worst-case local ambients) over the anticipated lifetime of the product.  | [1] 8.5 |  |
| 10.7 | ESD suppression component connections to the RF Reference (e.g. screws, rivets, conductive epoxy, solder, wires, conductive gaskets, etc.) must be reliably low-resistance over the anticipated lifetime of the product, taking into account shocks and vibrations, oxidation of metal surfaces, galvanic corrosion, temperature fluctuations causing movement due to different temperature coefficients, etc.  |  |  |

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|  Reducing emissions of mains harmonics and voltage fluctuations |
| *General Approach:* Either purchase a power converter that *really does* meet the specs needed, or design your own by using appropriate circuit techniques. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 11.1 | Purchase power supply subassemblies or modules that comply with the mains harmonics and voltage fluctuation standards (and all the other EMC and safety standards) that the product must comply with. | See 3.6 in this checklist |  |
| 11.2 | If necessary for compliance with a mains harmonic emissions standard, e.g. IEC/EN 61000-3-2, apply one or more of the detailed AC/DC power converter design techniques described in [1]. | [1] 10 |  |
| 11.3 | If necessary for compliance with a mains voltage fluctuations and flicker emissions standard, e.g. IEC/EN 61000-3-3, apply one or more of the detailed AC/DC power converter design techniques described in [1]. | [1] 11 |  |

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|  Protection from AC Mains supply Power Quality issues |
| *General Approach:* Either purchase a power converter that *really does* meet the specs needed, or design your own by using appropriate circuit techniques. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 12.1 | Purchase power supply subassemblies or modules that comply with the mains harmonics and voltage fluctuation standards (and all the other EMC and safety standards) that the product must comply with. | See 3.6 in this checklist |  |
| 12.2 | If necessary for compliance with power quality immunity test standards, e.g. IEC/EN 61000-4-11, -13, -14, -16, -27, -28, etc, use one or more of the techniques described in [1]. | [1] 12 |  |

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|  Heatsinks |
| *General Approach:* Return stray heatsink currents with very low impedance to the circuit(s) they came from, to help stop the heatsink acting as a resonant antenna. |
| **Good EM Engineering Practice** | **References** | **How applied** |
| 13.1 | Provisions must be made to RF-bond heatsinks to the RF Reference as close as possible to the device they are cooling, and control their shapes, to reduce their efficiency as “accidental antennas”. | [1] 13.1-7[2] 8.5 |  |
| 13.2 | Consider incorporating each heatsink into a local shield for the device(s) it is cooling. | [1] 13.8[2] 8.5.4 |  |

#  References and other sources of information

**[1]**  ***EMC Design Techniques for electronic engineers***, published by Nutwood UK November 2010, ISBN: 978-0-9555118-4-4, only available from www.emcacademy.org/books.asp

Alternatively, see the series of articles ‘**Design Techniques for EMC, 2006-9 series**’ posted on www.emcstandards.co.uk for free download.
Coursenotes and Webinars on these topics will also be available for purchase from www.emcstandards.co.uk during 2017.

**[2]**  ***EMC for Printed Circuit Boards – Basic and Advanced Design and Layout Techniques***, Nutwood UK, December 2010, ISBN 978-0-9555118-5-1, only available from www.emcacademy.org/books.asp www.emcstandards.co.uk

Alternatively, see the series of articles ‘**Basic and advanced EMC design of PCBs, series 2004-5**’ posted on www.emcstandards.co.uk for free download.
Coursenotes and Webinars on these topics will also be available for purchase from www.emcstandards.co.uk during 2017.

***The First 500 Banana Skins***, 500 reports and anecdotes of real-life interference incidents, ranging from amusing, through costly, to deadly. Very useful for convincing managers that EMC is a real issue that often costs companies large amounts of money. Only available from: www.emcacademy.org/books.asp

***EMC for Product Designers, 4th Edition***, Chapter 11, by Tim Williams, Newnes, December 2006, ISBN: 0-750-68170-5,
www.elsevier.com/books/emc-for-product-designers/williams/978-0-7506-8170-4

**Keith Armstrong’s webinars**

Visit: www.interferencetechnology.com/webinar-series or: www.youtube.com/user/InterferenceTech1, for:

* Cost-effective EMC Design by Working with the Laws of Physics
* Understanding EMC Basics (a 3-part series)
* Cost Effective Use of Close Field Probing (a 2-part series)
* PCB Suppression of ICs with BGA or Multiple Power Rails
* Cost-Effective Use of HDI (microvia) PCB Technology

And for: “Simulators for SI, PI, EMC can minimise / eliminate design iterations, and justifying their high cost is easy”, visit:
http://db.emclive2015.com/simulators-si-pi-emc-can-minimizeeliminate-design-iterations-justifying-high-cost-easy

**EMC assessment and testing:**

EMC Testing (in seven parts), ‘Do-It-Yourself’ testing from lowest-cost to fully accredited, by Keith Armstrong and Tim Williams, EMC & Compliance Journal,
2001-2002, posted on www.emcstandards.co.uk for free download as ‘DIY EMC testing series 2001’.

Assessing an EM Environment, Keith Armstrong, from the ‘Publications & Downloads’ pages at www.cherryclough.com

On-Site (in-situ) EMC Testing, Keith Armstrong, from the ‘Publications & Downloads’ pages at www.cherryclough.com

Guides on 17 different EM phenomena and their EMC tests, Keith Armstrong, REO (UK) Ltd., all posted on www.emcstandards.co.uk for free download under ‘EMC testing’.

**EMC for systems and installations:**

EMC for Systems and Installations, Tim Williams and Keith Armstrong, Newnes 2000, ISBN 0-7506-4167-3, www.bh.com/newnes,
RS Components Part No. 377-6463, cost around £40

Good EMC Engineering Practices in the Design and Construction of Fixed Installation, REO (UK) EMC Guide booklet, written by Keith Armstrong,
free download from www.emcstandards.co.uk.

Good EMC Engineering Practices in the Design and Construction of Industrial Cabinets (relevant for all types of electrical/electronic equipment),
Keith Armstrong, REO (UK) Ltd., free from: www.emcstandards.co.uk.

Complying with IEC 61800-3 – Good EMC Engineering Practices in the Installation of Power Drive Systems, by Keith Armstrong, published by REO (UK) Ltd.,
free from: www.emcstandards.co.uk.

Mains Harmonics (problems and solutions), by Keith Armstrong, REO (UK) Ltd., free from: www.emcstandards.co.uk.

Power Quality (problems and solutions), by Keith Armstrong, REO (UK) Ltd., free from: www.emcstandards.co.uk.