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Bench testing individual PCBs for immunity

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Bench testing individual PCBs for immunity

— to reduce financial risks

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Why should we bench-test individual PCBs for immunity?

First, a story to set the scene.

Way, way back in the mists of time, in 1981, I was an analogue circuit designer, and had worked my passage from junior to senior.

At that time, all I did was design circuits that were assembled onto individual printed circuit boards (PCBs), working to electrical, mechanical, functional and cost specifications that I had been given for that PCB.

I tested my circuits as “breadboards” and then as prototype PCBs on my test bench, using DC power supplies and laboratory test equipment. When the prototype met or surpassed its specifications, I signed off the drawings and they went into production at Issue 1.

Other people took my PCBs and integrated them into products, which were quite large items of equipment often containing several hundred PCBs, and these products were integrated in their turn into systems and installations.

I used to wonder why it was that circuits which worked so well on my test bench, often suffered from unacceptable levels of noise and/or distortion when first integrated into a product. The product integrator would have to fiddle around for days, maybe weeks, with the product’s cabling and construction to achieve its functional specifications.

Then when the product was integrated into a system, the same thing happened – the system integrator/installer would have to fiddle around for days, maybe weeks, to achieve the functional specs that I had already proved my circuits met – *on my test bench*.

Later on, when the system or installation was modified, the circuit’s noise performance would sometimes degrade again making it necessary to fiddle around once again, to recover the original specification.

Well, every circuit designer in that industry had the same issues with their circuits, and I was no worse than anyone else, so this terribly time-consuming and financially very risky process (outlined in Figure 1) was considered normal.

I would sometimes wonder why, for some PCBs, I had to reconfigure the “earthing” on my test bench to achieve the noise figures in the spec. But we all did that. We were paid to design circuits that met their specs when tested individually, and that is what we did.

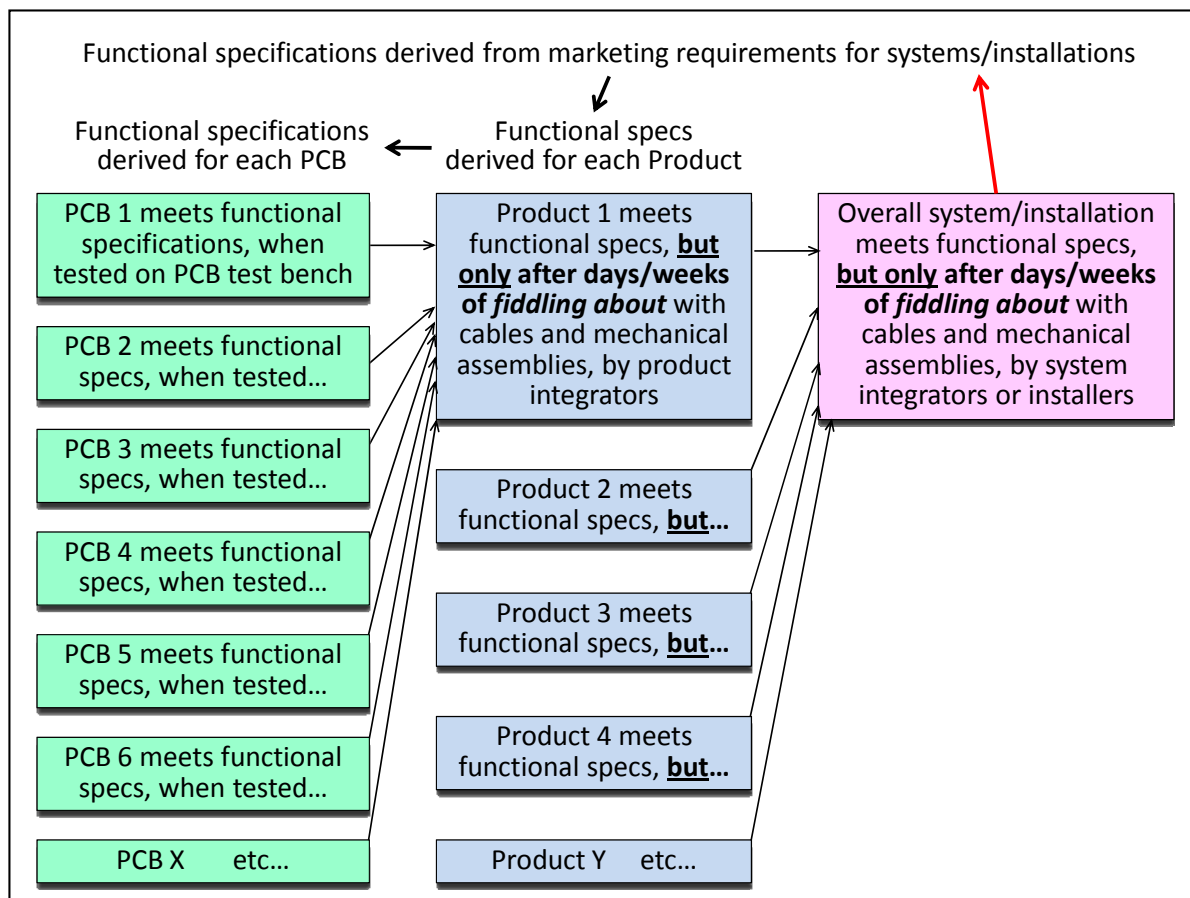
Since mid-1981 I have learnt a great deal about the reasons for the above. Because the company I worked for at that time was in a financial hole and making losses, it had been decided that its products needed to reduce their cost of manufacture dramatically, and a range of new circuit design, assembly, power distribution and signal cabling technologies were specified by a senior manager.

The first of this new type of product had 50 or more different PCB designs, some of them repeated 64 or more times. As usual, all the individual PCB types fully met their functional specs on their test benches – but the product’s overall functional performance on those same measures was truly *abysmal*. Noise, distortion, crosstalk, were all worse than the PCB specifications by 60dB, sometimes more.

No amount of the usual “fiddling about” by our very experienced product integrators made any impact at all, and I was told to find the solution, working on the first complete prototype of the product (which was intended to be the first actual product delivered to a customer, already well overdue).

After a week or two I had discovered what was wrong, visited the senior manager who had specified the new design and construction approach and showed him that very simple calculations that would fit on the back of a (small) envelope *proved* that products designed to his specifications would have exactly the *abysmal* functional performance we were getting, even though all their individual PCBs

would fully meet their specs when tested on their test benches. He merely shrugged and gave me a



small smile.

Figure 1 How it used to be (and often still is)

I then had to redesign the system, and (with several colleagues) redesign, re-prototype and retest every one of the 50 or more PCBs to suit it. Then I re-integrated them in the newly constructed product and showed that it now met its functional specifications. This took about 6 months, and the resulting delay in bringing the new product to market harmed the company's reputation. The company failed a few years later from this and other causes.

End of story.

I have since learned that the reason for all the fiddling about at each stage of integration was because of a mistaken understanding of how currents flowed. Everyone else in that industry (and most others) was making the same mistakes at that time, and many are still.

These mistakes are associated with the idea that alternating currents flow "downhill" until being absorbed by an "earth" or "ground" – that an "earth" or "ground" can be used as some sort of perfect waste disposal system for electrical signals and noise. It is pure imagination – there is no physical law that even *hints* at supporting such a view of current flow.

Many designers of circuits, products, systems and installations still make sure they have an "earth" or "ground" on their electronic schematics, for reasons of circuit operation and/or EMC rather than safety. Many designers of electronics for cars and airplanes treat their vehicle's "chassis" as if it was one of these impossible current-guzzling "earths" or "grounds".

Very many magazine articles, and even some conference papers and textbooks, have been written about how best to connect electronics to "earths" or "grounds", for functional or EMC reasons. They could all be described as works of fiction, although a better description might be that they are a shared hallucination – albeit one that has lasted for at least 6 decades and is still going strong.

In my EMC training courses, articles, papers and books for more than 15 years, I have strongly recommended that the words "earth" or "ground" – and symbols for them – are *never used* on electronic schematics, except where they are required for electrical safety (and then only for that purpose).

For a correct understanding of how currents flow (including strays such as CM currents) – and what this means for “earthing” or “grounding” – see [1] or [2] or Chapter 2 of [3], and [4]. If you prefer an academic understanding based solely on Maxwell’s equations, read the first chapters in [5].

My story above is only one of very many examples of huge delays and huge financial losses caused by this misunderstanding of how currents really flow. I know of *very* many more, and meet them all the time in my work as an independent EMC consultant.

Conversely, a correct understanding how currents (including “strays”) *really* flow, and how to design accordingly, makes it (almost) ridiculously easy to deal with most signal integrity (SI), power integrity (PI) and EMC design issues, at PCB, module, product, system and installation levels.

But this is getting away from the purpose of this article, which is that – when bench-testing a breadboard or prototype circuit – the real electromagnetic environment (usually abbreviated to EME) of the individual PCB should be applied (or simulated reasonably well).

In the above story, if we had followed what I propose below, the inadequacy of the product’s overall design would have been revealed before any significant project investment. The solutions I found would have been quickly and easily discovered, and most likely the new range of products delivered on time and without the huge cost over-run and harm to reputation that actually occurred. It is perhaps too much to believe that this would have saved the company, but it would certainly have helped!

A PCB’s EME includes all the *simultaneous electrical “noises”*, both radiated and/or conducted, that it will be exposed to by its intended product(s), system(s), installation(s) and the geographical location(s) where it will operate; plus all of the electrical, physical and mechanical issues associated with it, including details of its mounting, enclosure, cabling, and the proximity of other PCBs and objects.

Testing a breadboard or PCB on its own, using standard bench power supplies and test instruments, *cannot* tell us *anything* about its likely functional behaviour in real life, when integrated into a product, system or installation.

When all the PCBs that go into a product meet their functional specifications when bench-tested in a way that closely simulates their real-life EME, successfully integrating them into the new product will only take as long as it takes to assemble the product and perform its verification tests. There will be almost no risks to the project timescales or costs from this late project stage.

Therefore, the answer to the question posed by the title of this section, is that we should do immunity bench-testing of individual PCBs to save time and cost overall, and eliminate almost all of the financial risks from the product integration stage.

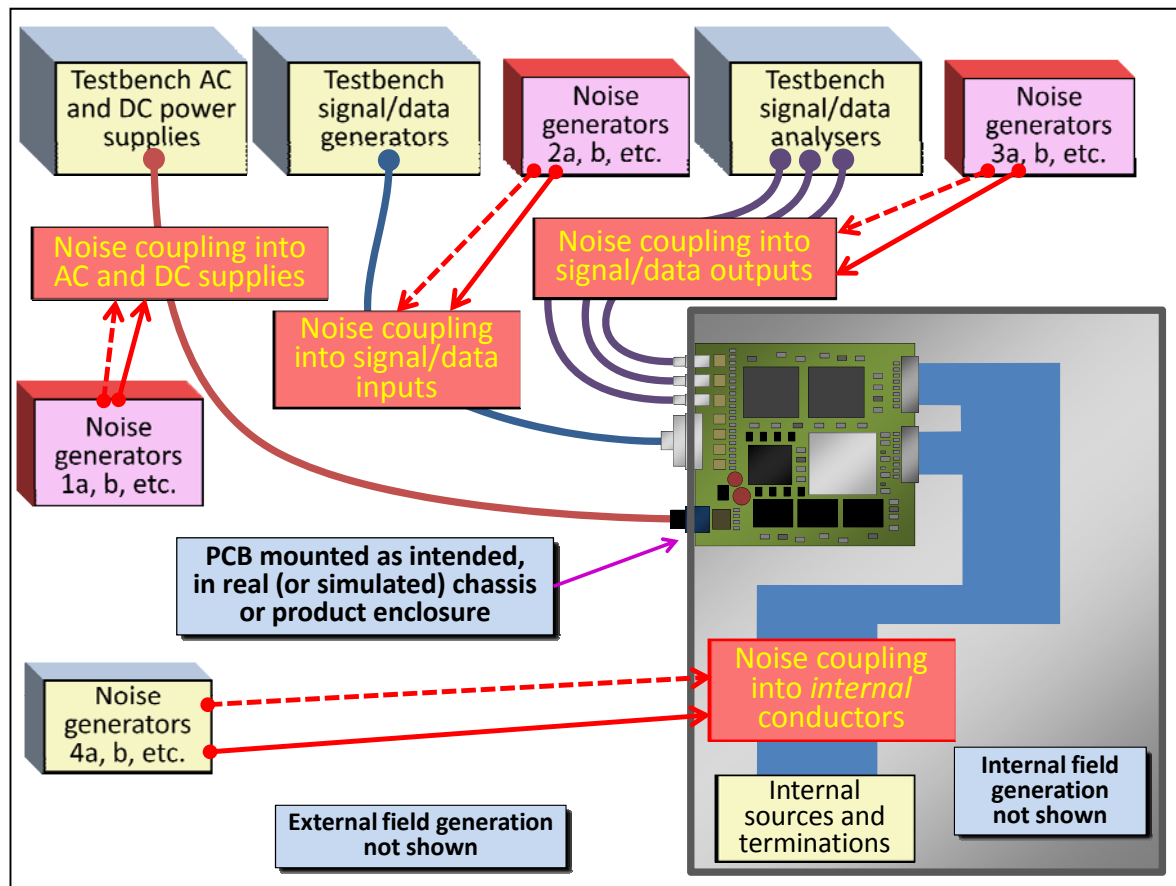
(There is often an additional benefit, in that PCBs designed and bench-tested like this generally achieve better SI and more robust software more quickly, helping to reduce time-to-market, improve market reputation, and justify higher selling prices.)

Product functional testing should simulate the EME of the systems or installations they will be used in. The usual EMC immunity tests make a stab at this, but for standardisation and repeatability requirements force a set-up that could be unlike the product’s real-life EME, and use tests that are unlike its real-life EME. That topic is outside the scope of this article, but most of the guides on doing EMC tests in [6] have a chapter on how to modify/extend the usual EMC tests so that they are closer to “Testing As Real Life” (TARL). Understanding what the external EME really is, for a given application, is of course vital when starting off this process, and [7] provides a useful guide.

Where errors or malfunctions in electronic circuits or software could possibly increase safety risks, the usual design and test approaches for compliance with EMC standards, directives or regulations are inadequate and IEC 61508:2010 plus IEC TS 61000-1-2 Ed2:2008 should be applied in full. The IET’s guide on EMC for Functional Safety [8] provides a great deal of practical advice on this, including checklists that can be used to control and audit the process.

How should we bench-test an individual PCB for immunity?

Figure 2 gives the general idea – the usual testbench instruments and AC/DC power supplies are passed through noise coupling circuits to connect to the PCB, which is assembled in a simulated product enclosure (if the real one isn't available). Various noise sources also connect to the coupling



circuits, to put realistic noises onto the power, signal, control and data cables.

Figure 2 General overview of bench-testing a PCB for immunity

There are various ways of coupling noise into cables, as shown in Figure 3. We can of course purchase coupling devices, but between 150kHz and 1GHz we can make them ourselves quite easily, and calibrate them (if we want to) with an RF generator and spectrum analyser or oscilloscope that covers the frequency range we are interested in.

The standard conducted immunity tests, for example IEC/EN 61000-4-4, -5, -6, and -16 specify how to design appropriate “coupling-decoupling networks” (CDNs), bulk current injection (BCI) and other coupling devices. These are most suitable when coupling noise into cables that will be external to the product, so will be tested with such networks in the final product compliance tests. The ISO 11452 series (automotive EMC), MIL STD 461F and DEF STAN 59-411 (military EMC) include some additional coupling methods that may be useful or more appropriate.

The coupling techniques described by standards like these may be more sophisticated than required when testing a product's *internal* EME. For example, in Figure 2, coupling the noise from generators 4a, b, etc. onto internal conductors – sometimes all that is needed to couple a noise generator's voltage into a wire, is a small capacitor.

If a testbench signal generator or analyser has a problem with the injected noise, we may only need to clip one or two RF suppression ferrites at its input or output. However, some signal analysers are very susceptible indeed to RF noise on their inputs, and may need to use a “proper” CDN or other standard-specified coupling device.

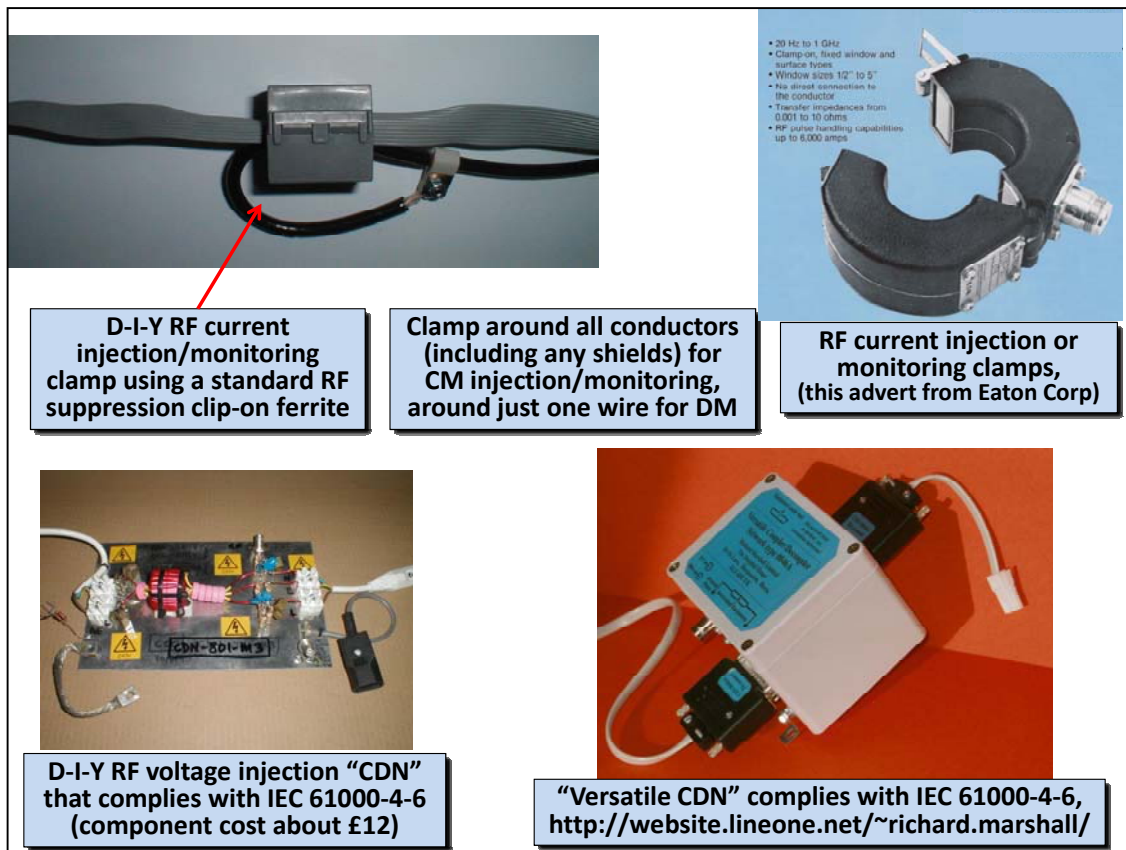


Figure 3 Some examples of conducted coupling devices

Figure 2 doesn't show external or internal radiated field generation, but there are a number of manufacturers of "desk top" striplines, TEM cell and small "anechoic" test chambers, and if we feel like saving cost we can make our own, see Figure 4.

If our product will have a shielded enclosure, and we are confident that we've got the shielding specifications right, we could instead test the PCB using only conducted external noise injection, and test the shielded enclosure separately with radiated fields to prove its shielding performance against external fields.

A problem with shielded enclosures is that – at their cavity resonance frequencies – internal fields will be magnified, maybe 100 or more times (+40dB) than what would occur with an unshielded product enclosure, possibly causing significant crosstalk that would never appear on a normal bench test. So when the product uses a metal box it can be very important to simulate realistic internal RF fields. The best simulators are the PCBs and devices that will generate the fields in real life, but if we don't yet have them we can use small internal antennas driven by external RF power amplifiers (the antenna's coax braid always connected to the enclosure wall with a bulkhead coaxial feedthrough connector).

The radiation efficiency of an antenna is strongly affected by the RF reflections inside a metal box, making it difficult to ensure the correct RF energy is being "launched" inside the box at all frequencies. However, AET's spherical dipoles (see Figure 4) can be used in a "levelling loop" with an RF power amplifier to generate the specified fields at their location.

Low frequency external and internal fields, say up to 1MHz, can easily be generated by small coils, and checked with other coils, using the formulae in the guide on IEC 61000-4-8 from [6].

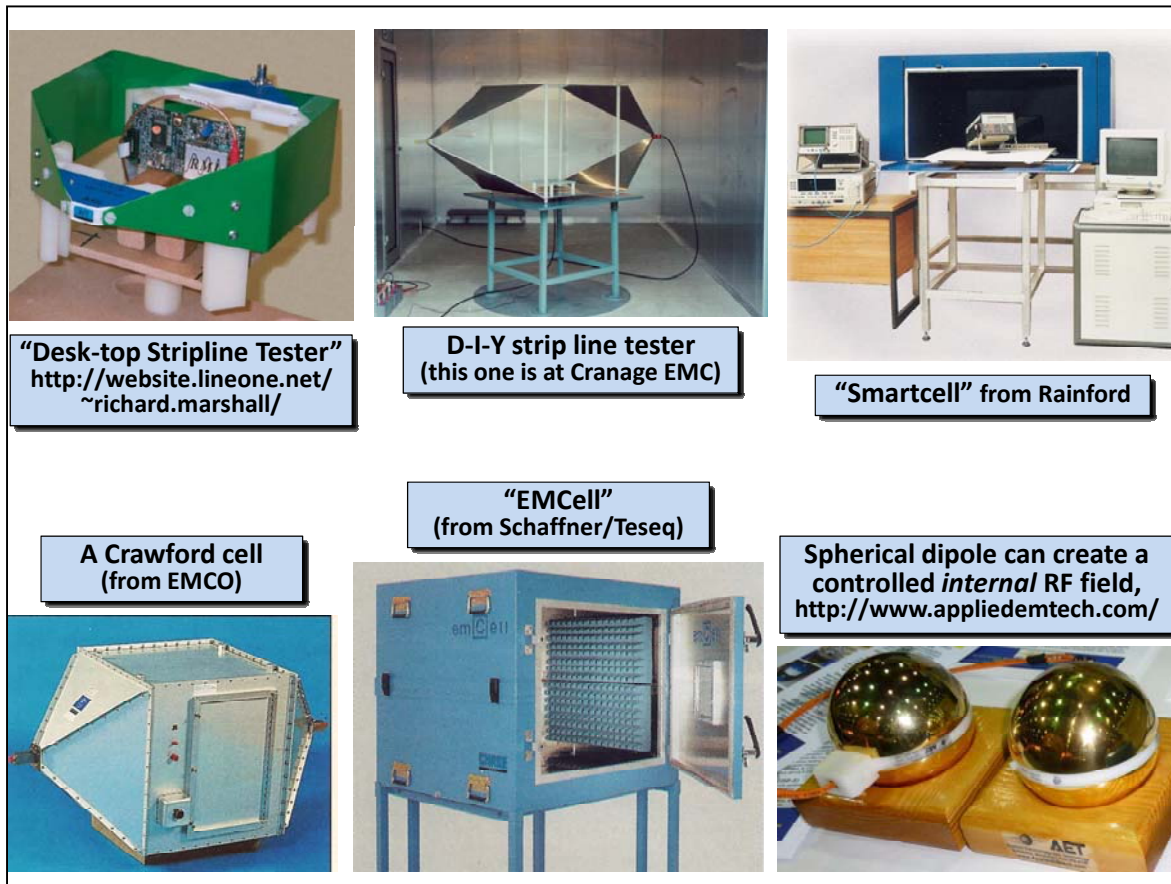


Figure 4 Some examples of radiated coupling devices

It's not as hard as it seems, and there's a lot to gain

Remember the two aspects to realistically simulating a PCBs' EME, mentioned earlier?

- a) All the electrical "noises", both radiated and/or conducted, that the PCB will be exposed to by its intended product(s), system(s), installation(s) and geographical location(s) where it could be operated, tested all at the same time.
- b) All of the electrical, physical and mechanical issues associated with the PCB, including details of its mounting, enclosure, cabling, and the proximity of other PCBs and objects.

These issues are discussed in more detail below, and they can seem quite overwhelming at first. However, like everything in electronic engineering there is a learning curve, and after the first such analysis has been done the subsequent ones get progressively much easier, and for a given range of products using a certain set of design technologies a considerable amount of "cut-and-pasting" will become possible. Also, obtaining/making/setting-up the noise generators and coupling devices will take some time and cost initially.

After a year or two you will wonder why you ever thought it difficult, and marvel at how much time and effort this approach would have saved, if it had been used on earlier projects.

It is important for the analysis of the EME bench-test requirements for each PCB is done very early in any project, so that the resulting bench-testing specification is an input to the design process. Then the designer can design accordingly, maybe using low-cost design techniques that are easy to design-in, but would be much more difficult to implement when the design had progressed to prototype stage.

At this stage in this sort of discussion, electronic designers usually start to complain about how hard this new approach is, and how much work is involved – as if this was a valid reason for ignoring the harsh financial realities of modern product manufacturing. Electronic engineering is hard to do quickly *and* well, and gets harder every year. Get used to it, or find an easier career (like managing hedge funds).

Usually, designers complain that their managers would never accept the extra time/effort/cost – but this only reveals that they are unable to effectively communicate the real needs of

design/development to their managers. This is not the criticism of design engineers that it seems – it is really a criticism of their education and training.

In most manufacturing companies the management is entirely focussed on financial matters, and very concerned indeed about investment payback periods and financial risks. Unfortunately these are not subjects that design engineers are taught about, so we end up with managers not understanding design engineering and imposing rules on engineers that make no real engineering sense and will actually result in financial harm. (A good example is the excessive focus on component cost, see [9]).

Design engineers are the only people capable of bridging this communication gap, because understanding how to do cost-effective product design is *at least* 1,000 times more difficult than understanding a project's (really rather simple) financial issues. Plus, the needs of design change with every cycle of integrated circuit die-shrinks (i.e. about every two years, according to Moore's Law).

If, as a design engineer, you *don't* want to make the effort to communicate what you need to improve your employer's financial success, you just want to keep your head down, do what you are told no matter how stupid it is, thinking you can blame the resulting mess on your managers (in fact, they will blame you, even if it was not your fault) – and if you have read this far – I urge you to change your approach. It is not hard for an electronics design engineer to learn to talk to managers in the financial terms they understand, and huge corporate and personal benefits are there for the taking! A good starting point is provided by [9] [10] and [11].

Electrical “noises”

Examples of the noises that a PCB is typically exposed to all the time in normal operation include (but are not limited to):

- Conducted differential-mode (DM) and common-mode (CM) noises on any power, signal, data or control input or output cable(s) *external* to the product, which connect directly to the PCB, caused by:
 - external ambient noises coupling to the external cable(s)
 - the operation of other equipment connected to the cable(s)
- Conducted DM and CM noises on the PCB's *internal* AC or DC power supply rail(s), which connect directly to the PCB, caused by:
 - external ambient noises on the product's AC or DC power supply cables that have not been completely attenuated by the product's power supply filter and conversion circuits
 - the operation of power AC and DC supply converters and power regulator circuits
 - the operation of other loads connected to the same power supply rail(s)
- Conducted DM and CM noises on any signal, data or control input or output cable(s) *internal* to the product, which connect directly to the PCB, caused by:
 - stray coupling from the magnetic and electric fields inside the product
 - the operation of other product circuits connected to the cable(s)
- Stray electric field, magnetic field and electromagnetic field coupling direct to the PCB's components and traces, from fields present in the product's *external* ambient that are not sufficiently attenuated by the product's shielding.
- Stray magnetic and electric field coupling direct to the PCB's components and traces from other PCBs, wires, cables, busbars, heatsinks, transformers, etc. *inside* the product.

When we don't know what internal noises to expect, we can measure the noises created by early prototypes of PCBs, or in a similar product that uses similar technologies (maybe even a competitor's product, if we intend to use the same ICs, PCB design, assembly techniques, etc.). Alternatively, it is increasingly cost-effective to model them using a computer field solver.

We need to know the noise amplitudes (voltage and/or current), frequency rates and waveshapes, and the tools we use are probes (voltage, current, and close-field types) with oscilloscopes and spectrum analysers. Remember that probe and instrument bandwidths need to have a bandwidth that is at least 0.35 times the reciprocal of the rise/fall time, to measure them at all accurately (e.g. 1.75 GHz, to measure 0.2ns).

The bench tests should apply the various noises *simultaneously*, because this is how they occur in real life. Ordinary immunity testing for complete products applies the various types of tests one at a time, which is not realistic and can lead to problems in the field. Very little immunity testing has been

done on simultaneous EM disturbances, but [12] shows that simultaneous immunity tests easily cause immunity problems even when a product passes all of the tests if they are done one-at-a-time.

It is easy to see why this can happen, taking the example of a digital processor. Its designers will have striven to keep the systematic, self-generated noises in its circuitry below its logic threshold by an amount called the “noise margin”. External noises that disturb the digital signals will “use up” a portion of the noise margin, and to avoid over-engineering most designers would aim to just about pass each type of EMC immunity test, meaning that the additional signal noise from each test used up almost the full noise margin on its own. Now, when two disturbances occur together, there is a chance that their combined noises will exceed the noise margin, causing software glitches and other malfunctions.

Unlike most (but not all) external EMEs, all of the various types of noise in the self-generated EME *inside* a product are almost always continually present, so simultaneous *internal* interferences are the usual situation.

Electrical, physical and mechanical issues

Here, we are concerned with all the “stray” couplings associated with a PCB and its assembled components, and the cables or other conductors that connect to it.

For example, a PCB will have a very different immunity to the electrical noise it is exposed to, if it is close to a large metal chassis, other metal object, cable, PCB, etc., depending on how it is electrically connected (or not) to that chassis, object, cable, PCB, etc.

Its immunity will also vary depending on exactly how the shields of any attached shielded cables are terminated (or not), at one or both ends, and whether its various connecting wires are twisted or not.

The outputs of AC and DC power converters should be loaded properly. If in real life a DC/DC converter will supply 3.3V at 10A to a PCB that has 100 off 100nF multilayer ceramic decoupling capacitors, via 300 mm of twisted-pair wire routed close to the chassis, then don't test it with a 3Ω 50W resistor soldered to its connector pins. Instead, put the resistor and 10μF of multilayer ceramic capacitors on the end of 300mm of twisted-pair routed close to the chassis like it will be in the product. Otherwise the RF stability of the converter, and the common-mode RF noise currents it generates, will not be tested.

Driving a CMOS gate input on a different PCB, over a length of wire, is not the same as leaving its output connector pin open-circuit. It requires the same length of the same type of wire, routed as it will be in real life, connected to a 3 or 4pF capacitor that is connected to its local 0V reference (usually connected to a different part of the chassis where that PCB will be mounted) to simulate the CMOS gate's input capacitance.

3pF has an impedance of 53Ω at 1GHz, lower still at higher frequencies, hardly something that can be ignored. And the capacitance of its wire to the chassis or other metalwork will usually be much higher than 3pF.

If the analogue signal or digital data being generated or analysed by the circuits on the tested PCB will in real-life be carried by a 2m-long ribbon cable along with 49 other signals/data, don't use just a single short conductor for it. The stray capacitance and inductance, and the crosstalk in the ribbon cable would not be present and the measurements would be misleading. Use 2m of the correct type of ribbon cable and put in it all the 0V and power conductors and equivalents to the other signals/data on the correct conductor numbers (sometimes just one signal or data used 49 times can be used, and often represents a worst-case scenario for crosstalk).

Those readers familiar with computer simulation of the signal integrity or EMC of product assemblies, will know that more accurate (i.e. realistic) results are obtained the closer the details of the simulated system correspond to real life. It is exactly the same with this methodology, which could be thought of as “hardware simulation”.

In fact, it is possible to perform computer simulations of circuits that are not yet available as prototyped PCBs, to discover what DM and CM electrical noises they will create, that need to be generated and coupled – whether radiated and/or conducted – in the bench-test of a prototype PCB assembly as shown in Figure 2.

Saving time during testing

Sweeping sine-waves over ranges of frequencies is very time consuming, and time can be saved by using “time-domain” test stimuli instead. Since the real-life noises in a product's external and internal EMEs are complex waveforms anyway, testing with similar waveforms is also much more realistic.

For example, switch-mode power converter noise is a series of pulses with harmonic content up to 1000 times the basic switcher frequency, so to simulate this – use a conducted noise coupling method to inject the output of a digital pulse generator to each DC power rail, in both CM and DM. Set it to pulse at the switcher frequency rate with pulse-width and rise/fall times corresponding to the expected switching waveforms. Suitable digital pulse generators that will switch in under 10ns can be bought new for under £1,000 (e.g. TG 5011, which will also provide analogue and arbitrary waveforms to over 10MHz).

It would, of course, be much more realistic to power the PCB from a prototype of the actual DC power converter it will use in real life – assembled and cabled in the PCB's chassis as it will be in the final product. There's no finer simulation than the real thing!

If the DC rail also powers digital circuits on other PCBs, simulate their noise with fast-edged narrow pulses at the clock frequency(ies). There's no need to use a digital pulse generator test instrument, simply make a digital clock generator (or as many as required) and couple its (their) their clock-buffered square-waves in CM and DM onto the DC rails, using low-value capacitors. Simply vary the value of a capacitor to increase the voltage noise being injected.

Where a noise has an unknown frequency, or frequency rate – and testing the range of possibilities would take too long – time can be saved by injecting noise only at the PCB's most susceptible frequencies. There are three kinds of susceptible frequencies:

1. Due to circuit operation, e.g. the full range of any analogue amplifier (test at the frequency at which the sensitivity is the highest); the frequency of any oscillator (analogue or digital) and all of their even and odd numbered harmonics. Can usually be determined by inspection.
2. Due to the resonances of mechanical, pneumatic, hydraulic, etc. sensors and transducers. Can usually be determined by analysis or simple tests.
3. Due to electrical resonances in cables, PCB traces, electrical/electronic components or circuits. Usually best determined by simple voltage or current injection tests over a frequency range, looking for peaks or troughs in the response of the item being injected into. Injection can be direct, taking care not to load the circuit and alter the resonant frequency, or indirect, e.g. by close-field probes.

Beware, RF current clamps often have enough inductance and stray capacitance to alter a conductor's resonant frequency. Resonance detection techniques such as described in [13] and [14] can be very powerful, for PCB traces, cables or any conductive structures, of any dimensions and over any frequency range.

Conclusion

Design and bench testing of individual PCBs as outlined above, to meet detailed specifications for their realistic internal and external EMEs, is a very powerful way of de-risking the integration stage of a new product project. Chapter 1.1 of [3] includes some worked examples that make this plain.

Even if the cost and time taken by this technique was the same as would be required to solve the problems in product integration that this technique should avoid (they will be less) – the corresponding financial risks to the project would be much lower.

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