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Avoiding imbalance in differential transmission lines on Printed Circuit Boards (PCBs)

Helping you solve your EMC problems

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Avoiding imbalance in differential transmission lines on Printed Circuit Boards (PCBs)

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EMERC = ElectroMagnetic Environment Research Center

Contents

Introduction

- **Differential signalling is being increasingly used in PCBs for high-speed clocks and data**
  - ➔ **because of their benefits for signal integrity (SI) and electromagnetic compatibility (EMC)**
    - ◆ **e.g. LVDS; PCI Express**
- **They use two traces driven with antiphase signals – usually called a 'differential pair'**
  - ➔ **these traces are designed and routed as *differential transmission lines* on PCBs**

'Single-ended signalling' is generated and received with respect to 0V (sometimes with respect to some other voltage reference instead) and uses one trace per signal. [1] describes the design of PCB transmission lines, and how to terminate them in matched impedances, for both single-ended and differential signals, and gives many other very useful references.

But differential signalling is increasingly required for clocks and communications (e.g. USB2.0, Firewire, Ethernet, PCI Express [2]) for both signal integrity (SI) and electromagnetic compatibility (EMC) reasons. [1], [3] and [4] are useful references for the general design of differential transmission lines.

Differential signalling uses two conductors driven with identical signals that are in antiphase with each other. Other names for differential signalling include 'symmetrical signalling' and 'balanced signalling', although these are more likely to be used in analogue circuit designs than in digital.

The result of well-realised differential signalling is better SI, lower emissions, higher immunity, and lower levels of ground and rail bounce noise on the signals output by ICs. LVDS (low voltage differential signalling) technology is becoming increasingly commonplace, and 'PCI Express' LVDS drivers have rise/fall times around 100ps.

Figure 1 shows two examples of differential signalling circuits. Sometimes + and – symbols are appended to the signal name to indicate a differential pair, instead of using a bar above one of them. A wide variety of differential transmission lines can be constructed using PCB traces and planes, as shown by Figure 2.

In an ideal world there would be no need for any electrical connection between the reference voltages for the driver and receiver. But in the real world the differential traces and their signals suffer from imbalances that give rise to common-mode (CM) noise, and connections between the reference voltages for the driver and receiver provide a return path for the resulting CM noise current – and so help reduce the EMC problems that it causes.

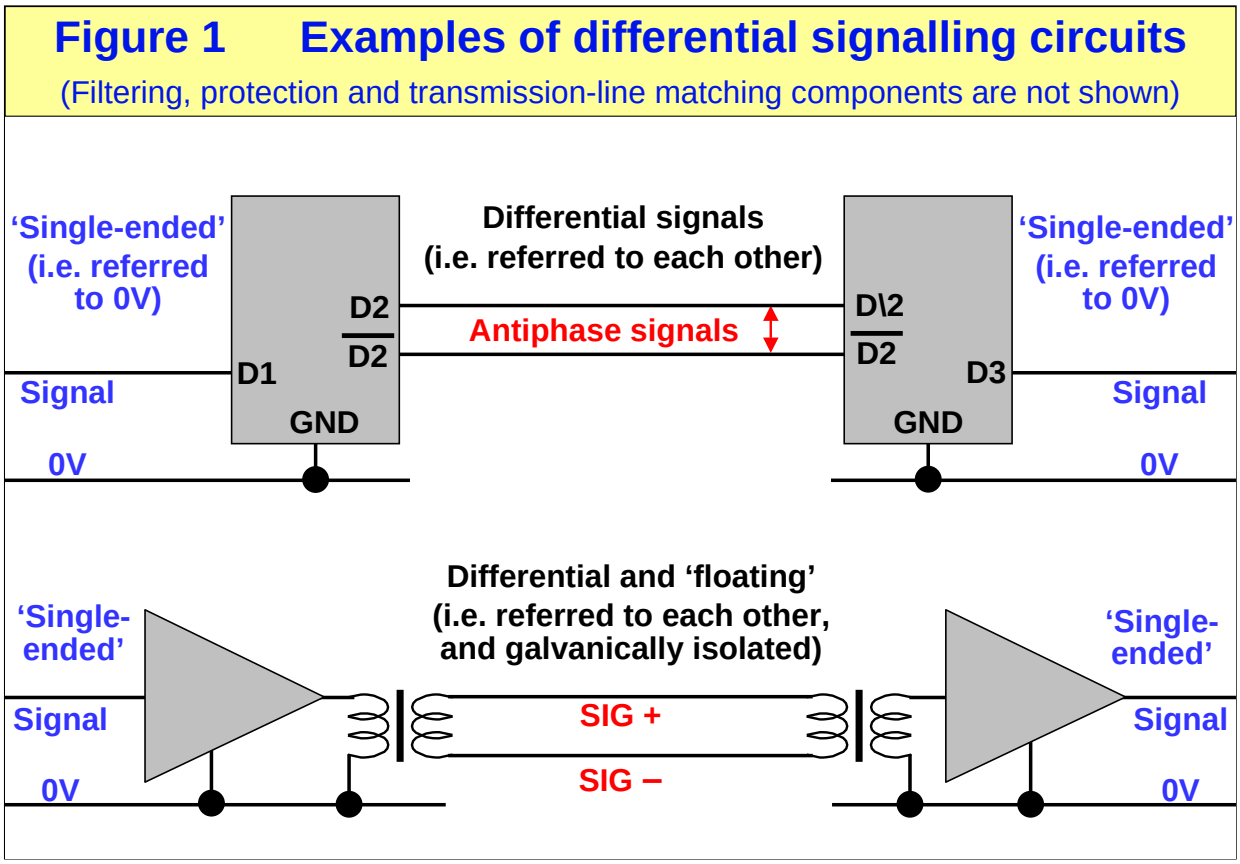


Figure 1

This figure shows two examples of differential signalling circuits.

Traditionally, digital differential signals use a bar above one of the signal names to indicate the inverted signal, but it is also common for + and – symbols to be appended to the signal names instead.

Other names for differential signalling include 'symmetrical signalling' and 'balanced signalling'.

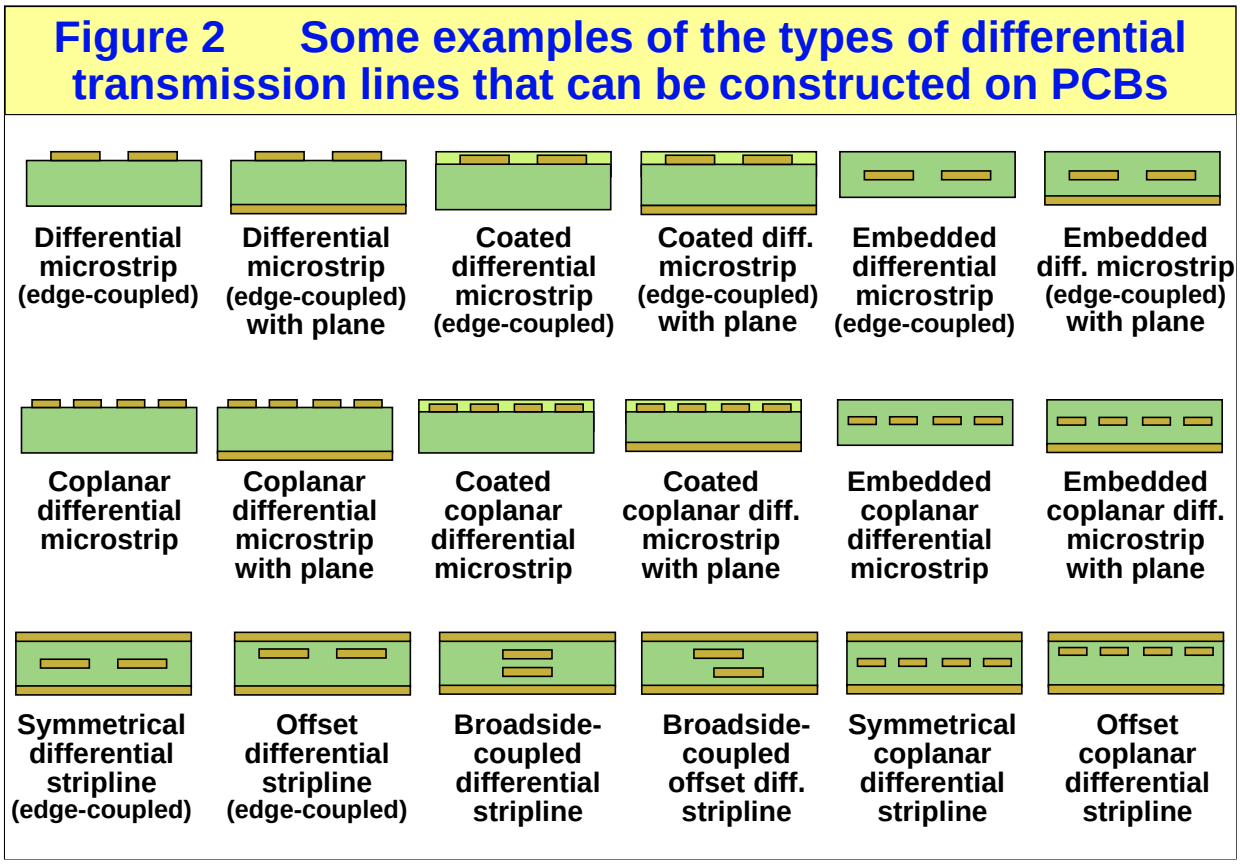


Figure 2

Some examples of the wide variety of differential transmission line structures that can be constructed using PCB traces.

Introduction continued…

- **But differential signalling suffers from *imbalances*, which cause…**
  - ◆**different waveshapes on each trace of the pair**
  - ◆**differential skew between each signal in the pair**

  ➔**each converts some of the differential-mode (DM) signal into unwanted common-mode (CM) noise…**
  - ◆**worsening EMC (both emissions *and* immunity), and SI**
- **Some causes of imbalance will be described…**

  ➔**as will some design techniques for controlling them, to help achieve good EMC and signal integrity (SI)**

The best EMC is created by very closely-coupled differential lines routed totally symmetrically along their entire route, with both their differential-mode (DM) characteristic impedance (Z_{0DM}) and their common-mode (CM) Z_{0CM} terminated in a matched impedance at one end, preferably at both ends. (When using LVDS it is often possible to use 'classical' termination (both ends termination) on a PCB by using sensitive types of LVDS receivers that accommodate a wide range of input levels.)

The SI and EMC benefits of differential signalling are reduced by any imbalances in the two antiphase signals and/or the traces used to create the differential pair.

Imbalances can create two kinds of problems, sometimes at the same time…

1) Waveshape imbalance (the shape of the + signal is not the exact inverse of the - signal)

2) Differential skew (the + and - signals are not perfectly synchronised in time)

Both types of imbalance cause some of the DM (wanted) signal current to be converted into unwanted CM noise currents. The worse the rate of conversion from DM signal to CM noise, the higher will be the emissions from the differential traces.

Figure 3 shows an example where only differential skew is present. In such a situation, a differential skew equal to X% of a signal's rise/falltime results in a CM voltage that is X/2% of the differential signal amplitude [5].

The same imbalance that causes the DM-CM conversion can take CM noise from the environment (e.g. a radio transmitter) and convert it into DM noise in the differential traces. DM noise is in the same mode as the signal, so it easily causes interference.

So we can say that a differential pair that suffers from imbalance and so has higher levels of emissions, will also have poorer immunity.

This presentation describes a number of causes of imbalance in differential signalling on PCBs, and also describes some design techniques for reducing imbalance to help achieve the maximum benefits from differential signalling, for both SI and EMC.

Figure 3 Differential skew converts some of the DM signal into common-mode (CM) noise

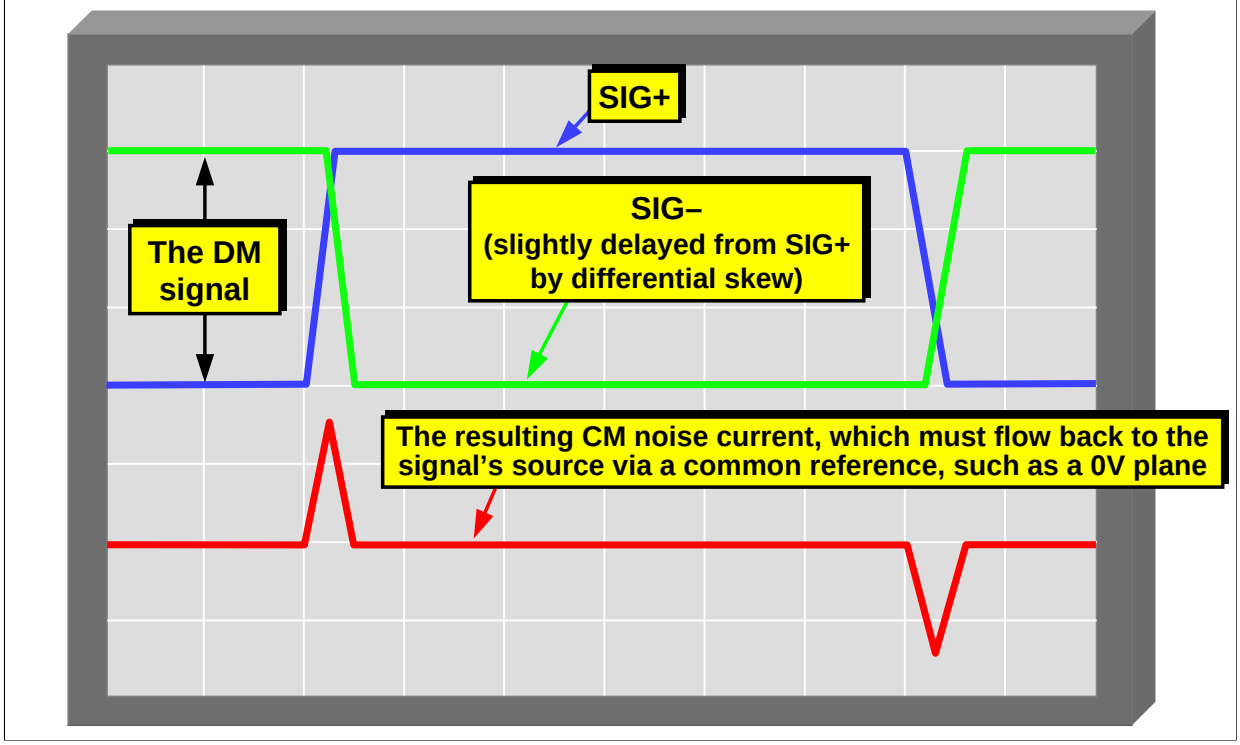


Figure 3

The worse the differential skew – the higher the levels of the CM noise currents created [5].

In other words, the worse the timing differences between the two halves of the differential signal – the higher the rate of DM-CM conversion, in which a proportion of the wanted DM signal gets converted into unwanted CM noise.

An increased rate of DM-CM conversion is bad for EMC emissions, and for immunity.

The effects of imbalance on differential signalling

- **The 'balance' or 'symmetry' of a differential pair should be maintained over its full length…**
  - ➔ **otherwise SI and EMC (emissions and immunity) will be made worse**
- **Where the CM return path is not perfect…**
  - ➔ **e.g. gaps or splits in a plane, or when the pair connects to a cable with imperfect shielding…**
  - ➔ **just 150ps of differential skew can make EMC as bad as a single-ended signal**

To maximise the benefits of differential lines for both SI and EMC, it is important to maintain their 'balance' or 'symmetry' along their entire routes. Guidance on this is given later in this presentation, and also in [2] (for PCI Express) and [6].

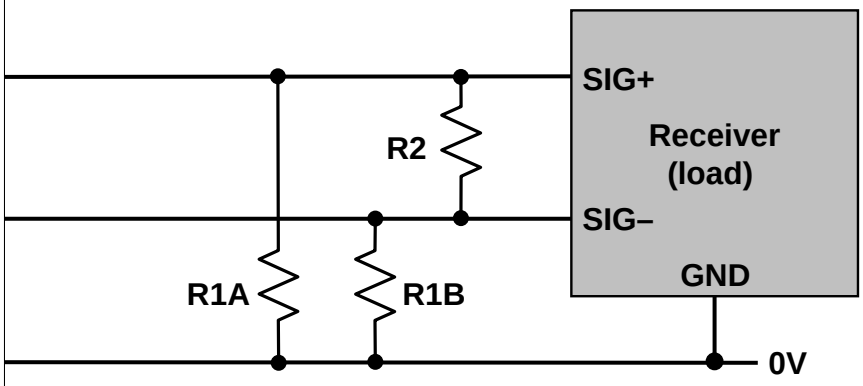
Where reference planes suffer from gaps, or where the PCB traces connect to shielded cables and/or connectors that do not use true 360° shield termination at *both* ends – then the CM current return path is not a good one. As a result, just 150ps of differential skew can degrade the EMC performance of a differential line so that it is no better than using 'single-ended' signalling with a single trace.

As the differential skew exceeds 10% of the duration of the shortest signal, it can start to affect the SI (for example, the data's 'eye pattern' will start to close).

Even where the differential signalling is entirely confined to a single PCB, and both of the traces are routed over an unbroken reference plane (usually 0V), imbalances can have a significant effect on EMC, and on SI – especially as data rates approach 10Gbps.

Figure 4 shows an example of the terminations that should be used with differential transmission lines to ensure that both the wanted DM signal and the unwanted CM noise are correctly matched, to prevent reflections and standing waves and obtain the best SI and EMC [2].

Figure 4 Examples of differential line terminations (using the 'incident wave switching' method)



R1A = R1B, chosen to match the transmission line's CM ('even order') characteristic impedance (Z_{0CM})

R2 in parallel with (R1A+R1B) matches the transmission line's DM ('odd order') characteristic impedance (Z_{0DM})

'RC', 'Thévenin' and 'Active' termination methods can also be used, as can reflected wave termination.

Classical termination (termination at *both* ends of the transmission line) is the best, but requires sensitive receivers

Figure 4

This shows an example of the terminations that should be used with differential transmission lines to ensure that both the wanted DM signals *and* the unwanted CM noises are both correctly matched – to prevent reflections and standing waves in either of them to help obtain good SI and EMC [1], [2].

Causes of imbalance

- ➔ **Unequal stray coupling to the traces**
- ➔ **Differences between the two trace widths**
- ➔ **Propagation time differences for + and - signals**
  - ◆ **e.g. caused by woven PCB substrates such as FR4**
- ➔ **Driver timing asymmetry**
- ➔ **Different driver impedances (pull-up versus pull-down)**
- ➔ **Coatings on microstrip traces**

There are a number of causes of imbalance, including…

- Unequal stray coupling to the traces
- Differences in trace widths
- Propagation time differences for the + and – signals
  (e.g. caused by path length differences; or by the use of woven glass-fibre PCB dielectrics)
- Driver timing asymmetry
- Different driver impedances (pull-up to pull-down)
- Coatings on microstrip traces

Each of these contributions is discussed in more detail in the following slides.

To help ensure that a PCB will not have significant EMC problems due to imbalance in its differential transmission lines, it is recommended that the designer sets an ‘imbalance quota’ for waveshape differences, and for differential skew, for each differential signal.

Ideally, these quotas would be set based on previous experience with exactly the same technology (chips, PCB structure, etc.) – or by doing experiments on a simple test PCB that is representative of the design techniques and ICs that are to be used, to see how much of each type of imbalance can be permitted.

Then during the PCB design the contributions from all of the above causes are individually quantified (see the references for the relevant equations) and added together.

If the total of all the contributions exceeds a quota limit, some or all aspects of the circuit or PCB design should be modified to reduce their effect, until the quota is no longer exceeded.

Using field solvers in conjunction with circuit simulators can help determine the imbalance quotas and the PCB structures that will help achieve them, see later.

Unequal stray coupling to the traces

- **Unequal stray coupling occurs when one trace in a pair is closer than the other to…**
  - **a gap in a PCB, or an edge**
  - **a gap in a copper plane, or an edge**
  - **an object (whether metal, glass, plastic, ceramic, etc.)**
  - **an area of copper fill pattern, or another trace**
  - **water, oil or other liquids**
- **Using stripline (ideally, coplanar stripline) helps 'shield' trace pairs from stray coupling**
  - **and using closely-coupled traces (routed very close together) also helps reduce stray coupling imbalance**

When a differential pair of traces pass near an object, one trace will generally have a different stray inductance and/or stray capacitance coupling to it than the other, unbalancing the line. Objects that can cause imbalance include:

- gaps in PCBs (i.e. an absence of dielectric), or the edges of PCBs
- gaps in planes, or the edges of planes
- objects made of metal, plastic, glass, epoxy, ceramic, etc.
- other traces, or areas of copper fill
- water (e.g. condensation), oil or other liquids

To help maintain a good line balance, each trace should be routed well away from anything that might cause imbalance. Ideally, keep either trace more than D/10 away from the edge of a plane of dimension D. Figure 5 shows some examples of stray coupling causing imbalance.

Recommended layouts for such situations can be found in application notes, articles and papers (e.g.[6]) – but most of these only concern SI. Balance that is good enough for EMC is much harder to achieve than it is for SI.

Stripline between two unbroken planes is best, with vias (or decoupling capacitors) linking the two planes at least every one-tenth of a wavelength ($\lambda/10$) over the whole PCB, at the highest frequency of concern. The width and spacing of the traces should remain constant along their route, and they should not route near or over any gaps or edges in the top and bottom planes.

The top and bottom planes shield the trace pair from all objects and gaps except those that occur in the same PCB layers (alongside the trace pair). Routing an outer 'return' trace, connected to one (or both) of the stripline planes, along each side of the differential pair helps to shield the trace pair from objects that occur within their PCB layer. This four-trace configuration is called a 'differential coplanar stripline'.

Note: The 'highest frequency of concern' can be calculated as $1/\pi t_r$ where t_r is the real risetime of the driver IC, *not* the maximum risetime specification from its data sheet.

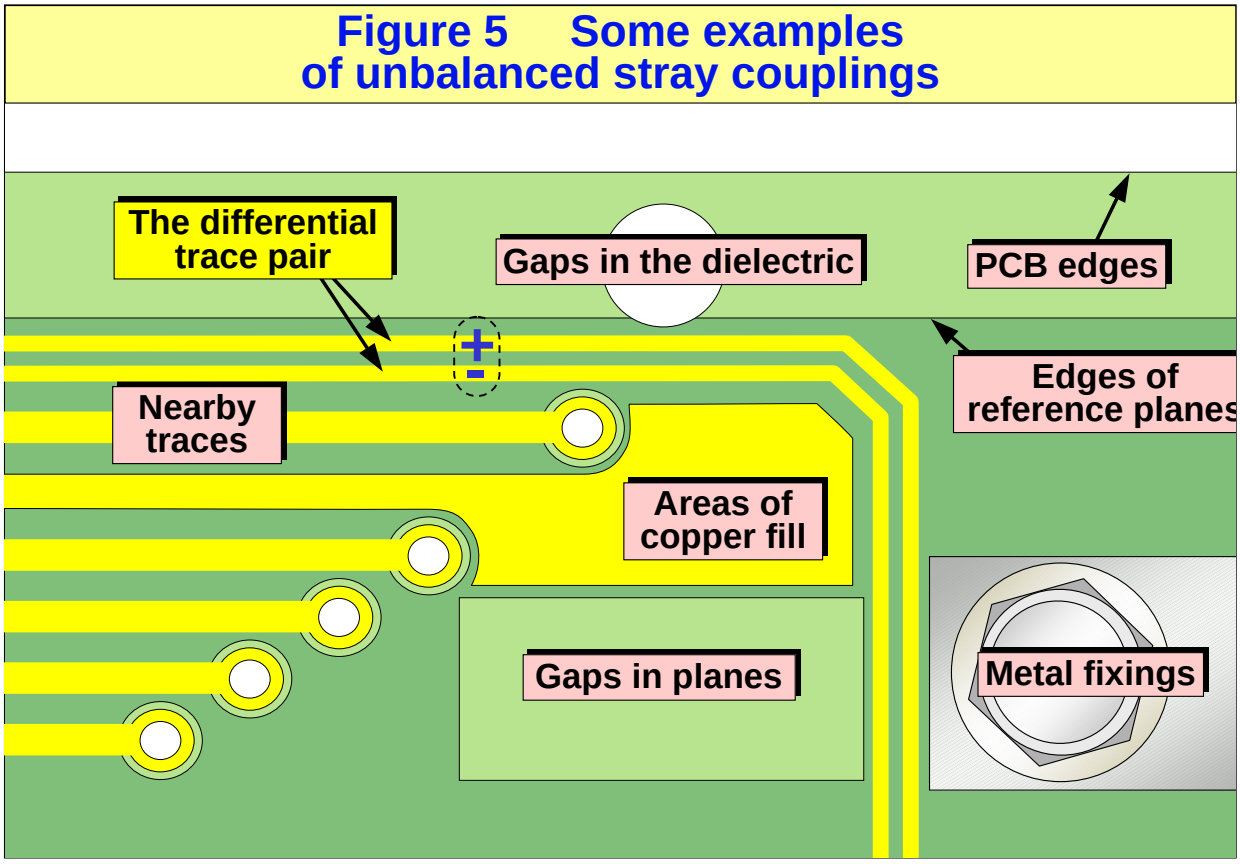


Figure 5

Some examples of typical features found on PCBs
– that can cause imbalance if they are near to a differential transmission line

Routing a differential pair through a dense field of via holes

- **It is best to route the trace pair symmetrically between the vias**
  - **using fine-line traces or microvia (HDI) PCB technology as necessary**
- **To minimise costs, it might be acceptable to…**
  - **vary trace widths to compensate for imbalances**
  - **increase the spacing between the traces to route only one trace between vias (but use symmetrical routing)**
  - **use broadside routing**

Maintaining the balance of a differential pair can be very difficult when it must pass through a field of closely-spaced via holes – for example under a BGA IC or a dense multiway connector. The best solution would be to use trace widths and spacings that were as small as they needed to be to route each pair symmetrically through the via field [7] – with a sufficient width of plane on an adjacent layer symmetrically located above and/or beneath the pair to carry their return currents [8]. But where this requires traces and spaces that are narrower than what is normally available, the costs of manufacturing the PCBs might increase.

Where the above techniques are not used, some design compromises may be required. It might be possible to compensate for a deviation in one trace (e.g. to pass around a via hole) by widening or thinning one of the traces. But where the traces in the pair are closely-spaced together (the best routing for EMC, especially where the CM return path is not ideal) – it might be difficult to maintain *both* DM Z_0 *and* CM Z_0 in this way.

Another compromise is to space the trace pair so far apart that their CM Z_0 is simply twice their DM Z_0 – then route them as individual traces along their whole route and through the field of vias. It is best to achieve an identical routing pattern for each of the traces in the pair, but the EMC will not be as good as if a closely-spaced trace pair was used.

Broadside routing routes the two traces in parallel on adjacent PCB layers, and is generally considered to be a bad idea [5]. But when routing through a field of vias, broadside routing at least allows the traces to maintain their relationship with each other whilst routing only one trace between each pair of vias on any layer – so it may be an acceptable compromise.

Figure 6 sketches some examples of the above techniques.

But the ideal solution for EMC reasons is to use microvia PCB technology instead of through-hole-plate (THP). Microvia is also known as high-density interconnect (HDI) or sequential build-up, and uses blind and/or buried vias with very small diameters. Because the vias are so small and do not have to penetrate every layer, there is more space available in the via field for routing trace pairs symmetrically. Where production volumes are sufficient it should be possible to find an HDI manufacturer who will charge the same (or less) as a THP PCB.

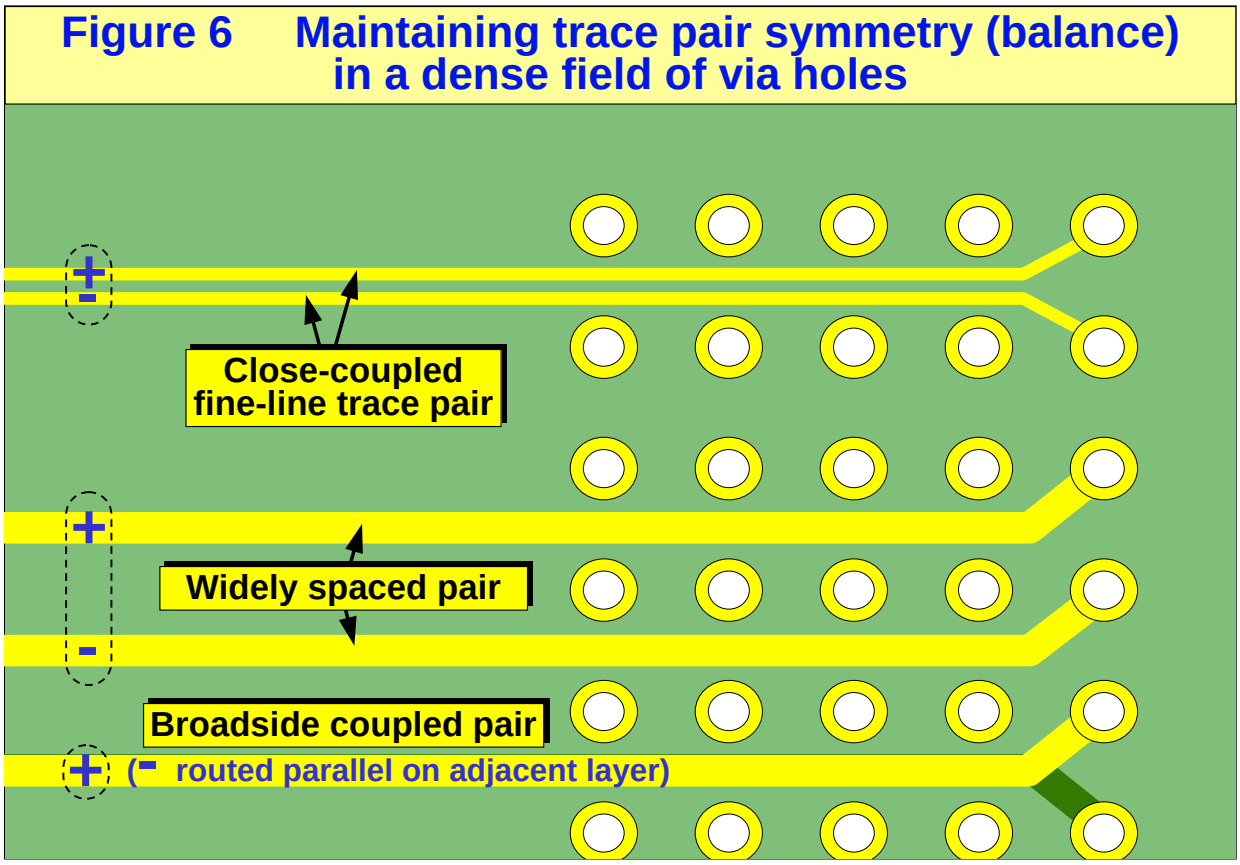


Figure 6

This figure shows some examples of routing differential transmission lines through a field of closely-spaced vias or pads, without losing their symmetry (balance).

The best method is generally to use trace width/spacing that are as narrow as they need to be to route two traces symmetrically through the via field [7]. If using coplanar differential lines, four traces will need to be routed symmetrically.

(Remember that when using thinner traces, the trace-plane spacing may need to be reduced as well to maintain the desired Z0.)

The preferred method for EMC is to use HDI (also called microvia or sequential build-up) instead of through-hole plate, to prevent BGA and similar devices from creating routing problems on all the layers beneath them. This technique is not shown above.

Differences in trace widths

- **Variations in trace widths can cause imbalance**
  - ➔ **can be caused by uneven manufacturing processes, and/or the limited resolution of the phototool**
- **Techniques for controlling trace width imbalance include…**
  - ➔ **placing two or more 'test traces' on the PCB, and testing their DM and CM Z_0 before accepting any batch of PCBs delivered by their manufacturers**
  - ➔ **routing critical traces at 20°- 70° to the phototool's digitisation grid**

Variations in trace width during PCB fabrication can be a cause of imbalance. These can be caused by process variations during manufacture (e.g. etch rate, plating rate) over the length or width of the PCB.

Errors in trace width and spacing can also occur depending on where they land on the virtual grid produced by the natural resolution of the phototool (e.g. Gerber).

For single-ended transmission lines the effect of erroneous trace widths caused by the above is usually only considered to be significant when trace widths that are less than 0.13 mm (5 thou). But for differential lines, the effect on line balance can be much more significant.

To control process variations it is best to include 'test traces' [9] at two or more widely-separated locations on a PCB, so that manufacturing quality can be checked at the Goods Receiving department as part of a goods acceptance procedure.

Testing differential line test traces requires the use of a 4-port vector network analyser. These used to be very specialist and expensive pieces of scientific equipment, but versions are now available, from manufacturers such as Polar Instruments [10], which are suitable for use by relatively unskilled staff in the Goods Receiving department.

But it is quite possible that PCB test traces would not detect trace width errors caused by the phototool resolution, for all of the traces. One way of helping to avoid imbalance caused by phototool resolution is to route all differential trace pairs at angles of between 20° and 70° with respect to the phototool's digitisation grid. This will tend to 'average out' any resolution errors along the length of a trace.

Propagation time differences for the + and - signals

- **Propagation time differences for the + and - signals cause differential skew directly**
  - ➔ **caused by differences between the trace lengths**
    - ◆ **and/or by differences in their propagation velocity V**
- **22mm path difference in stripline in FR4 can cause 150ps of differential skew**
    - ◆ **maybe as low as 11mm if there is capacitive loading**
  - ➔ **so where the CM return path is poor: trace lengths may need to be matched to between 2 and 1mm**

The velocity of propagation (V) for a stripline trace in FR4, without any components fitted to the PCB, is about 6.8ps/mm of trace length, whereas for a thin microstrip trace on FR4 V is about 5.5ps/mm.

But when the PCB is loaded with components, the additional capacitive loading caused by the devices will slow down the V. For a heavily loaded bus the capacitive loading can slow it to as little as half of the bare-board's V.

(But note that many applications of differential signalling are point-to-point, where the additional capacitive loading along the line is non-existent or very small.)

So, for example, 150ps of differential skew could be caused by between 11 and 22mm of path length difference for stripline traces in FR4, depending on their capacitive loading.

It was mentioned earlier that where the CM current return path is poor – just 150ps of differential skew can cause very significant EMC problems.

In such situations, to obtain significant EMC benefits from differential signalling we should aim for path length differences to be no more than about 10% of 150ps, between 1 and 2mm depending on capacitive loading. But this assumes that path length differences are the sole cause of differential signal skew. Since there are other contributions to the overall value of differential skew for a trace pair, the differential skew caused by path length differences should be even less than this.

Where the CM noise currents have a low-impedance return path that is in very close proximity to the differential signals along their entire route, larger path length differences may be acceptable for EMC.

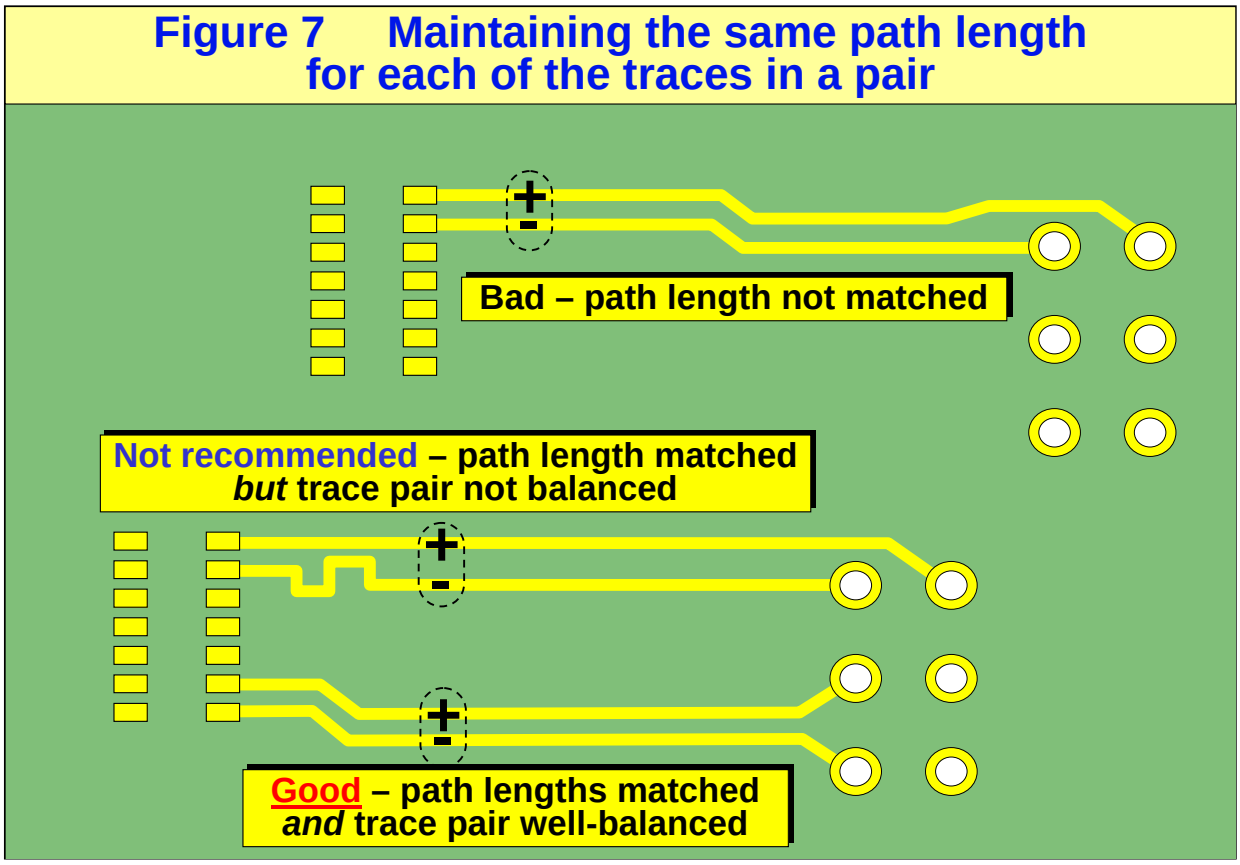


Figure 7

This figure shows an example of a path length matching problem caused by the poor allocation of pins in a connector.

The path length difference can be corrected by 'serpentining' the shorter trace, but this causes another sort of imbalance between the traces in the pair.

The best solution to this example is to reallocate the connector pins so that the trace pair can be routed symmetrically, and with the same path length.

Generally, connectors that are designed specifically for use with differential lines will have pin allocations that allow trace length matching to be achieved easily. These are the best types of connectors to use.

The effects of woven PCB dielectrics

- **Woven glass-fibre PCB dielectrics (like FR4) use glass-fibre with ε_r = 5.6 and epoxy resin with ε_r = 3.2 (both approx. values)**
  - ➔ **routing over a glass-rich region *reduces* Z_0 , V**
  - ➔ **routing over an epoxy-rich region *increases* Z_0 , V**
- **The resulting imbalance problems can be severe (as much as 5% of the line's propagation time)**
  - ➔ **but the problems can be reduced by routing at 30°-60° to the direction of the PCB's glass-fibres**

The glass-fibre used in popular PCB substrates (such as FR4, G-10, Nelco 4000-13SITM, Rogers 4350B, Polyclad FR-406, etc.) has a much higher dielectric constant than the epoxy resin. We normally assume that FR4 has a relative dielectric constant (ε_r) of 4.2, above 1MHz, but this is in fact the average of the high ε_r of the glass-fibre (about 5.6) and the low ε_r of the epoxy (about 3.2).

The glass-fibres used in PCBs are woven like ordinary cloth, with a 'warp' and a 'weft' (or 'fill') direction. When routing a trace close to the warp or fill direction, if it happens to lie predominantly in or over a glass-rich area – its actual Z_0 and V can be lower than were calculated assuming an ε_r of 4.2 [11]. But if instead the trace happens to lie predominantly in or over an epoxy-rich area, the Z_0 and V will be higher than was calculated assuming an ε_r of 4.2. See Figure 8.

The effect of the glass-fibre dielectric on the imbalance of a trace pair can be very significant [12] – the differential skew it causes can be up to 5% of the propagation time along the line.

The usual way of overcoming this problem (without using more costly non-woven dielectrics, see later) is to route the differential lines at angles of between 30° and 60° to the warp or weft of the glass-fibres in the PCB, so that the effect of the woven substrate tends to average out reasonably well [11].

Another technique is to make the spacing between traces in a pair equal to the spacing between the glass bundles in the PCB material, but although this will prevent imbalance between the traces in the pair – it will make the overall values for Z_0 uncertain and make the line difficult to match with the correct impedances, so this method is not recommended.

[12] shows that PCBs based on woven glass-fibre dielectrics will have serious difficulties with signals at 10Gb/s or more on traces longer than 600mm (e.g. in a backplane) even when using the above techniques. It has been proposed that, if woven glass-fibre dielectrics are to be used at such high data rates, electronic de-skewing techniques should be used in the receiver ICs. But although this would be a good technique for SI, it would not help EMC.

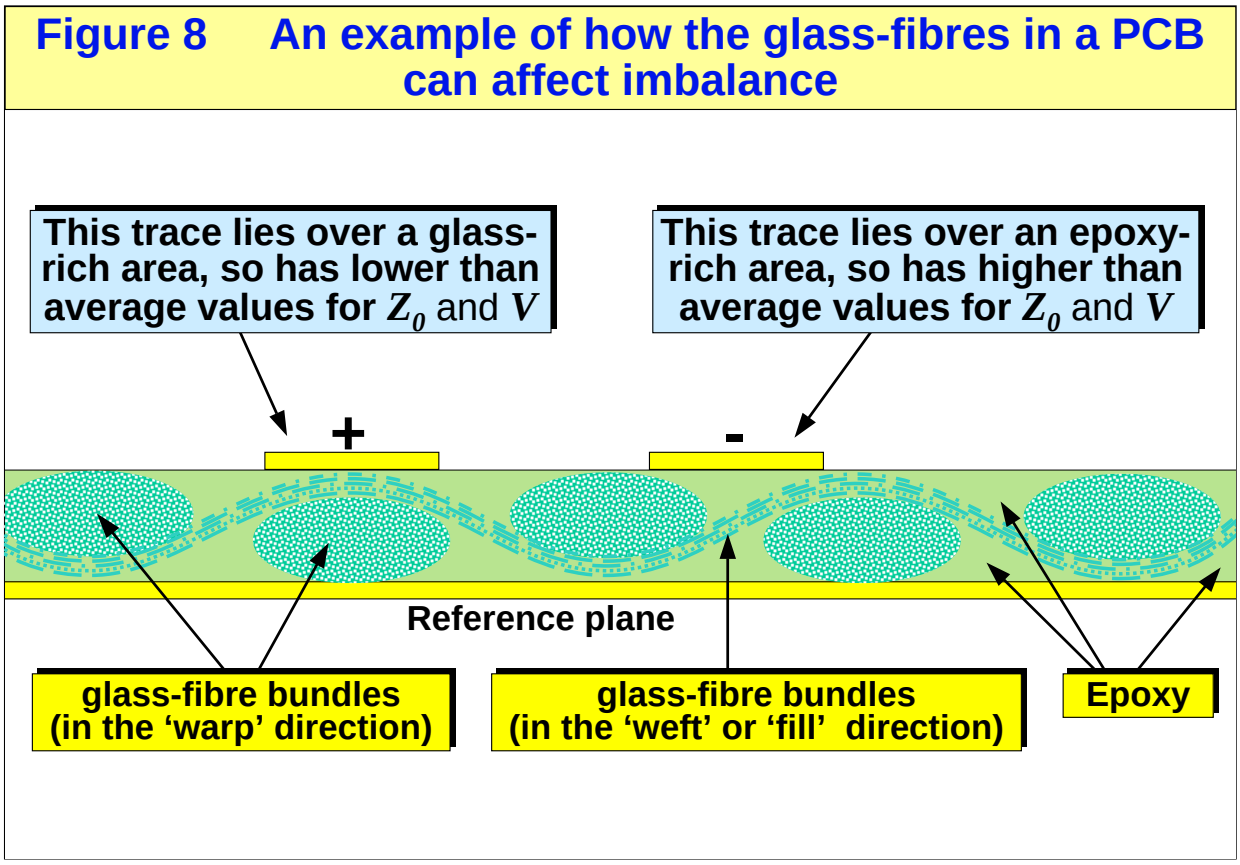
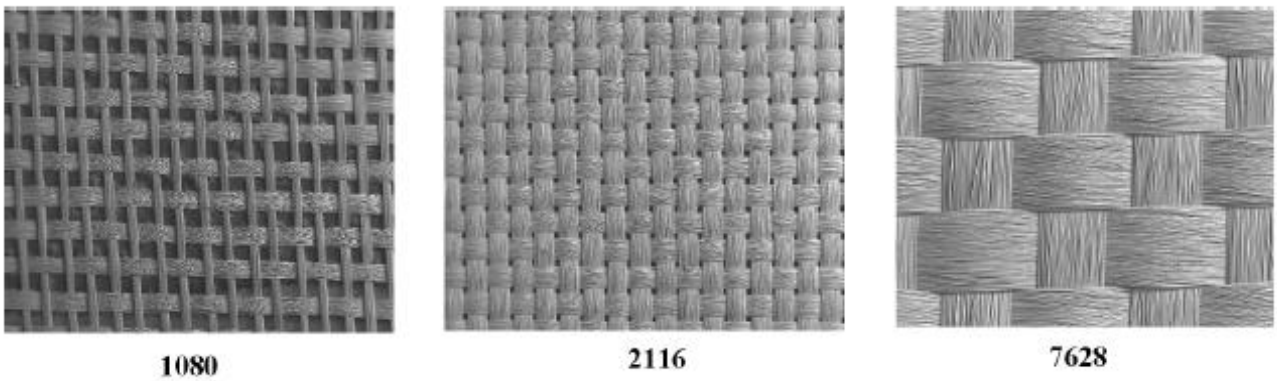


Figure 8

This figure shows a cross-section of a PCB, with its 'warp' and 'fill' glass-fibre bundles encapsulated in epoxy resin. The warp direction is perpendicular to the paper, so we see these glass-fibre bundles in cross section.

When traces are routed in the same direction as the warp or fill, they can lie over areas which have more glass-fibre than the average for the whole PCB, or else they can lie over areas which have more epoxy content than the average. Either situation causes an imbalance.

Figure 8B Some examples of the glass-fibre weaves used in PCB manufacture (from [12])



Using homogenous dielectrics

- **Homogenous dielectrics are good, but costly**
  - **they use non-woven materials, e.g. pure polymers**
- **To save cost, use just one or two homogenous layers in a PCB stack-up that is otherwise made of layers of low-cost woven glass-fibre dielectric**

➔**route the differential traces so that their Z_0 and V are governed by the homogenous PCB layer(s)**

- **but make sure that the PCB manufacturer proves he can achieve good yields and PCBs that will be reliable over the products' lifecycles**

It has long been predicted that developments in high-speed devices and circuits would mean that FR4 and similar low-cost woven glass-fibre PCB dielectrics would be replaced by homogenous dielectric materials (such as pure polymers). But although these materials are much better, they are also so much more costly that designers have found ways to keep on continuing to use the old low-cost dielectrics.

It seems likely that homogeneous dielectrics will become essential for differential lines as data rates approach (and exceed) 10Gbps.

Suppliers of homogenous dielectrics, sometimes called microwave substrates, include WL Gore and Rogers Corporation.

One cost-saving technique uses just one or two layers of a homogenous dielectric (e.g. WL Gore's "Speedboard C" prepreg [13], or GETEK [14]) in a PCB stack-up that is predominantly made using layers of FR4 or similar low-cost woven glass-fibre dielectric.

The PCB stack-up and routing ensures that the Z_0 and V of the differential trace pairs are governed by the homogenous dielectric layer(s), and relatively unaffected by the woven glass-fibre dielectric layers.

This technique only adds a little extra cost compared with the traditional alternative of using all homogenous dielectric layers in the PCB.

But not all PCB manufacturers may be able to successfully laminate these different materials and/or create reliable PCBs. Accelerated life testing may be required to feel confident that such mixed dielectric stack-ups will last the expected life of the product.

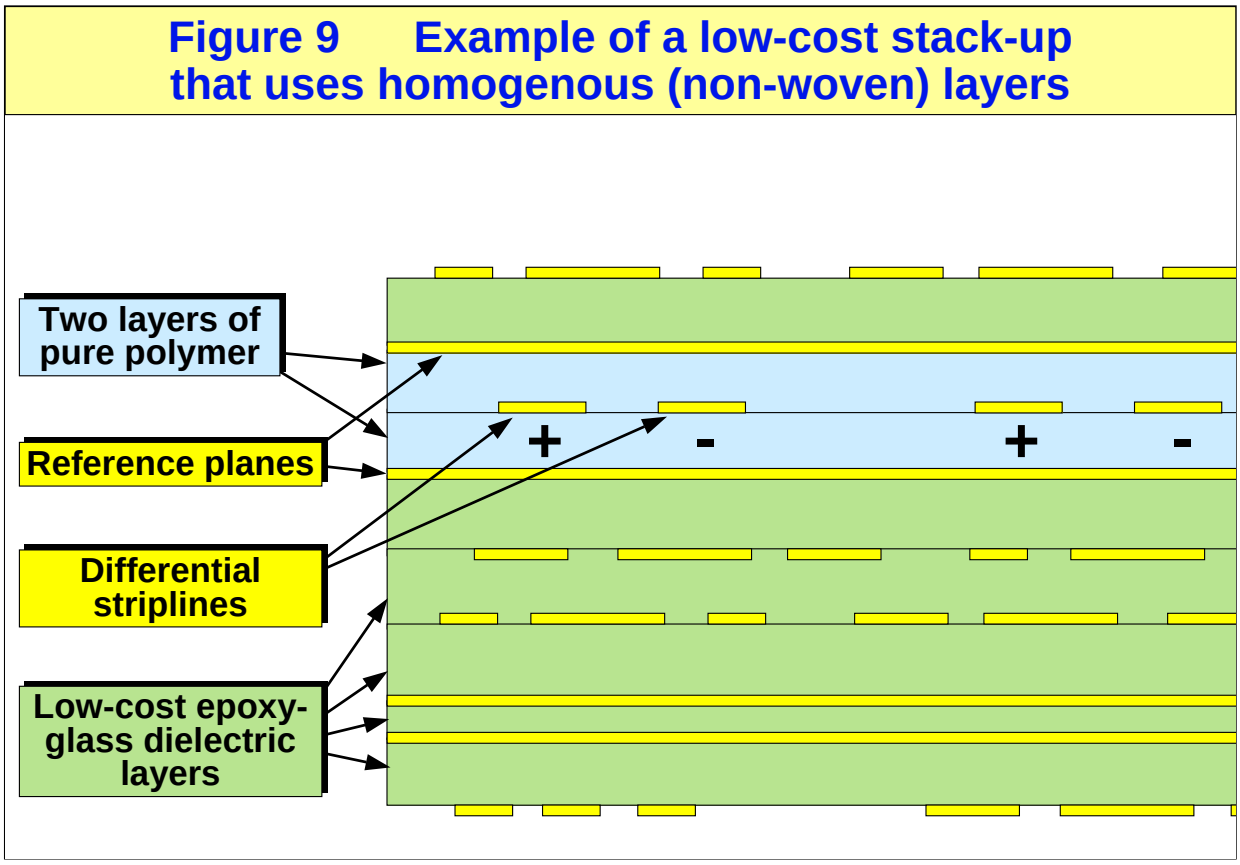


Figure 9

Some manufacturers can embed one or more layers of homogeneous dielectric (like the pure polymer in the above example) in a stack-up that is predominantly FR4 or some other low-cost woven dielectric.

The high-speed differential lines would be routed in the homogenous dielectric layers, to avoid the fluctuations in balance that can be caused by the glass-fibre bundles having a very different ε_r from the epoxy.

Driver timing asymmetry
(between the + and – signals)

- **Signal timing differences between the + and - outputs of the driver devices cause differential skew directly**
  - ➔**some devices have very poor specifications**
  - ➔**some have no specifications, or only 'typical' ones**
- **So always read the data sheets carefully**
  - ➔**and choose devices on the basis of their *maximum* differential skew specifications**

Better driver timing symmetry means that the + and – signals in the differential pair switch more nearly at the same instant (or in the case of sinewave signals, have less phase difference). The result is lower differential skew, which in turn means lower CM emissions and higher immunity.

So always check data sheets for maximum differential skew data. If it isn't in the data sheet – assume the specification is too poor.

If only typical differential skew figures are given for a device – don't rely on them.

Even if a device appears to have good differential skew when tested in a test jig or on a PCB – at some time in the future its manufacturer might start shipping devices that explore more of the 'specification space' permitted by his data sheet (see Chapter 15 of [15]) – so unless the maximum specification in the data sheet (or in a letter from the manufacturer) is good enough for a design, choose a device with a better specification.

For example, the data sheet for the DC90C031 LVDS Quad CMOS Differential Line Driver specifies its typical differential skew as 80ps, but its maximum as 900ps.

900ps is a huge value of differential skew – equivalent to about 120mm of trace length difference for a differential stripline – considerably more than the 150ps mentioned earlier.

A PCB using such devices would require great care in its EMC design to make sure that a batch of devices with differential skews at the highest permitted by their data sheet could not cause EMC problems.

Driver impedance asymmetry

- **Typical drivers have different output impedances when they are pulling up, compared with when they are pulling down**
  - **➔so the waveshapes of the + signals might not be the exact opposite of the - signals**
    - **◆depending on the traces they are driving**
  - **➔another cause of imbalance that leads to CM noise**
- **So it is best to choose drivers with low (e.g. 10Ω) and 'symmetrical' output impedances**

The outputs of ordinary ICs do not have identical impedances when pulling up and when pulling down. For example, a typical CMOS 'glue logic' IC can have an output impedance of 44Ω when pulling up, but 11Ω when pulling down. Also, the output impedances vary dynamically, depending on their voltage.

Unequal output impedances between pulling up and pulling down can make the waveforms of the + signals differ from those of the - signals. This means the waveshapes of the differential signals may not be exact opposites, and this imbalance causes some DM to CM conversion to occur – increasing CM emissions and worsening immunity.

Adding some series resistance at the driver end of the transmission line can help a little. For example, adding 22Ω at the output of the above driver would make its output impedance when pulling up 66Ω, and its impedance when pulling down 33Ω – only half of its original asymmetry.

However, it is much more effective to use devices containing drivers that are designed for driving transmission lines. These should have a low impedance (e.g. 10Ω) when pulling up or down.

Always check their data sheets (or ask their manufacturers) for the worst-case difference between the pull-up and pull-down output impedances – then use the devices that the specifications prove will be good enough in the actual PCB, taking all the other imbalances into account.

Problems with coated microstrips

- **Microstrip traces are usually coated with solder resists, 'silk screen' legends, etc.**
  - **the dielectric constants of these coatings are often unknown, or not very well controlled**
  - **➔and if they cover more of one trace than the other, or are thicker over one trace, this causes imbalance**
- **Best dealt with by design (e.g. no coatings over differential pairs)**
  - **➔or by detailed specification of coating materials, and/or batch tests of PCB 'test traces'**

There were some examples of coated microstrip PCB structures in Figure 2. The usual coatings are solder resists (solder masks) and component legends (sometimes called the 'silk screen' layer).

Some PCBs are 'conformally coated' to protect them from moisture or contaminants, and/or encapsulated to help protect them from shock and vibration.

But the dielectric constants and loss factors of many such coatings are not very well characterised at high frequencies, and the thickness of coating applied is often not very well controlled.

In addition, most PCB specifiers only specify the solder mask by its solder-resisting qualities, leaving the PCB manufacturer free to substitute various alternatives. This can cause variations in transmission line characteristics between different PCBs, and possibly over the width or length of a single PCB.

One way of dealing with this problem is to ensure there are no coatings or printed legends over any microstrip lines. Another way is to include a number of test traces (see earlier and [9]) at widely-spaced locations on the PCBs and test them against specific performance targets at Goods Receiving before accepting any batch of PCBs from its manufacturer.

Actually specifying the solder mask and legend materials by their manufacturers' part numbers should also help maintain quality.

Accidental coatings can also present problems. For instance condensation, liquid sprays and dust, especially if the dust is conductive. The dielectric constant of water is very high (around 80), and the deposition of condensation, liquid sprays and dusts tends to be very uneven, so the result is that these can be very important causes of imbalance.

Of course, striplines don't suffer from the problems of coatings, whether they are intentional or accidental, which is one reason why they are preferred over microstrip for good EMC for differential transmission lines.

‘Channelised’ striplines

- **Trace pairs can be shielded by placing ‘walls’ of via holes symmetrically along both sides…**
  - **➔with the vias connecting the top and bottom planes**
    - **◆and the vias spaced apart by less than one-tenth of the wavelength, at the highest frequency of concern**
- **This makes it easier to achieve a good balance**
  - **➔and the shielding also reduces the EMC impact of line imbalance from other causes**
    - **◆but does not prevent them from affecting SI**

A differential stripline can be ‘channelised’ by placing a row (or ‘wall’) of via holes along both sides of the trace pair. The vias connect to the planes that lie above and below the trace pair, so the planes must be at the same potential. The aim is to space the via holes so closely together that they create a shield for the differential stripline traces inside the PCB.

When using a coplanar differential stripline (four traces, see Figure 2) the via walls should follow the route of the return traces, connecting them to the top and bottom planes to create a shielded coplanar differential stripline.

To have a significant shielding effect, the via holes must be spaced no further apart than one-tenth of a wavelength at the highest frequency of concern. The smaller the spacing between the via holes, the better their shielding effectiveness.

It is important to route the via walls symmetrically on both sides of the differential pair so that good line balance is achieved. An unsymmetrical structure of traces, planes and vias would unbalance the differential line. Although the shielding that was created might prevent such imbalance from causing large EMC problems, signal integrity problems could be created.

‘Channelised’ differential lines are much less affected by imbalance due to stray coupling with nearby objects or gaps in planes and PCBs. But it is very important to maintain a symmetrical structure (when seen in cross-section) along the whole route of the trace pair.

The shielding effect of the via walls also improves the EMC of the differential line, so that CM emissions due to imbalance caused by other reasons (e.g. driver differential skew) will cause less emissions. Immunity is also improved. But please note that the shielding does not prevent imbalance from causing problems for SI.

The author has not yet seen any equations for calculating the Z_0 or V of a ‘channelised’ differential stripline – but they will both have lower values than when the via walls were not present. Accurate design would probably require testing an experimental PCB, or using a field solver (see later).

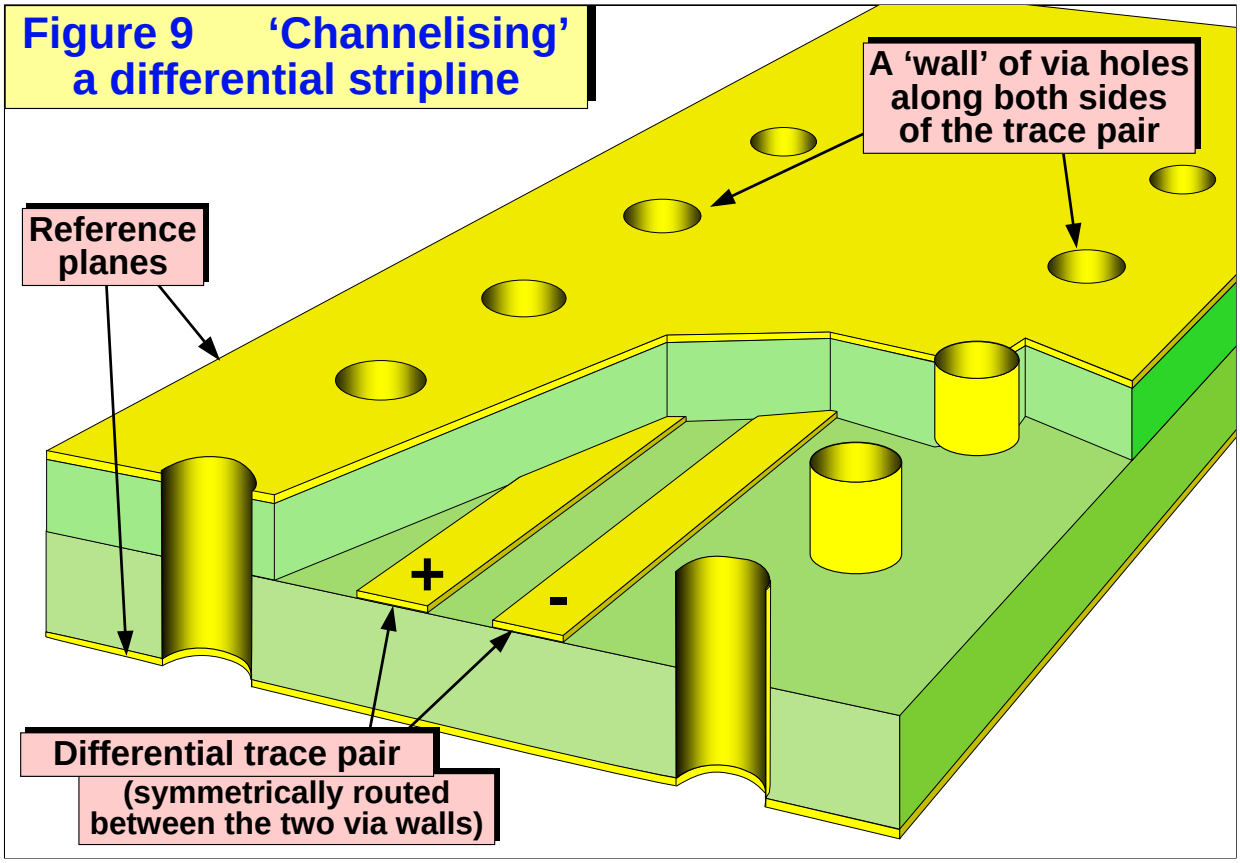


Figure 9

This shows a differential stripline (a trace pair routed between two reference planes) with symmetrically-routed rows of vias linking the two planes on either side of the trace pair.

This is often called 'channelising', and it provides a degree of shielding for the pair – helping to protect them from other features or objects that might unbalance them.

The amount of shielding achieved at any given frequency depends upon the spacing between the via holes (see the previous page).

The via holes will increase the capacitance seen by the traces, so they will have lower values of Z_0 and V than would be expected from the normal equations for differential striplines.

If using coplanar differential striplines, the via holes should be routed along the middle of the outside traces, linking them to the two reference planes at every via.

Shielded striplines

- **Some PCB manufacturers can create fully shielded traces inside a PCB**
  - ➔ **by cutting trenches and plating them with copper**
- **This provides better shielding performance than 'channelising' with rows of via holes**
  - ➔ **but must be symmetrical to maintain line balance**
  - ➔ **and the good shielding performance reduces the EMC impact of any remaining imbalances**
    - ◆ **but doesn't reduce their effect on SI**

Some PCB manufacturers can now create linear trenches between layers in a PCB, plate them with copper and fill them back up with epoxy, as shown in Figure 10. These can be used to create well-shielded transmission line traces inside a PCB [16] that have much better EMC than ordinary differential transmission lines can ever achieve.

This technique brings the same shielding advantages as channelising using rows of via holes on both sides (see the previous slide) – but should provide even better EMC performance because higher values of shielding effectiveness should be achieved.

Shielded differential lines are much less affected by imbalance due to stray coupling with nearby objects or gaps in planes and PCBs. And the impact of the remaining imbalance (such as trace length matching or woven dielectrics) on EMC will be considerably reduced – although their effects on SI will not be.

As for the channelised differential stripline discussed in the previous two slides, it is important that the shielding is symmetrical with respect to the differential traces along its entire route. An unsymmetrical shield would unbalance the differential line, and even if the shielding prevented this from causing EMC problems it would not prevent it from having an effect on SI.

[17] gives a formula for calculating the Z_0 of such shielded traces – but only for single-ended transmission lines. All equations suffer from simplifying assumptions, so might not achieve good enough matching for modern high-speed PCB interconnections. A field solver (see later) will give exact values for Z_0 and V.

Figure 10 Cross section of a PCB trace shielded by metallised trenches

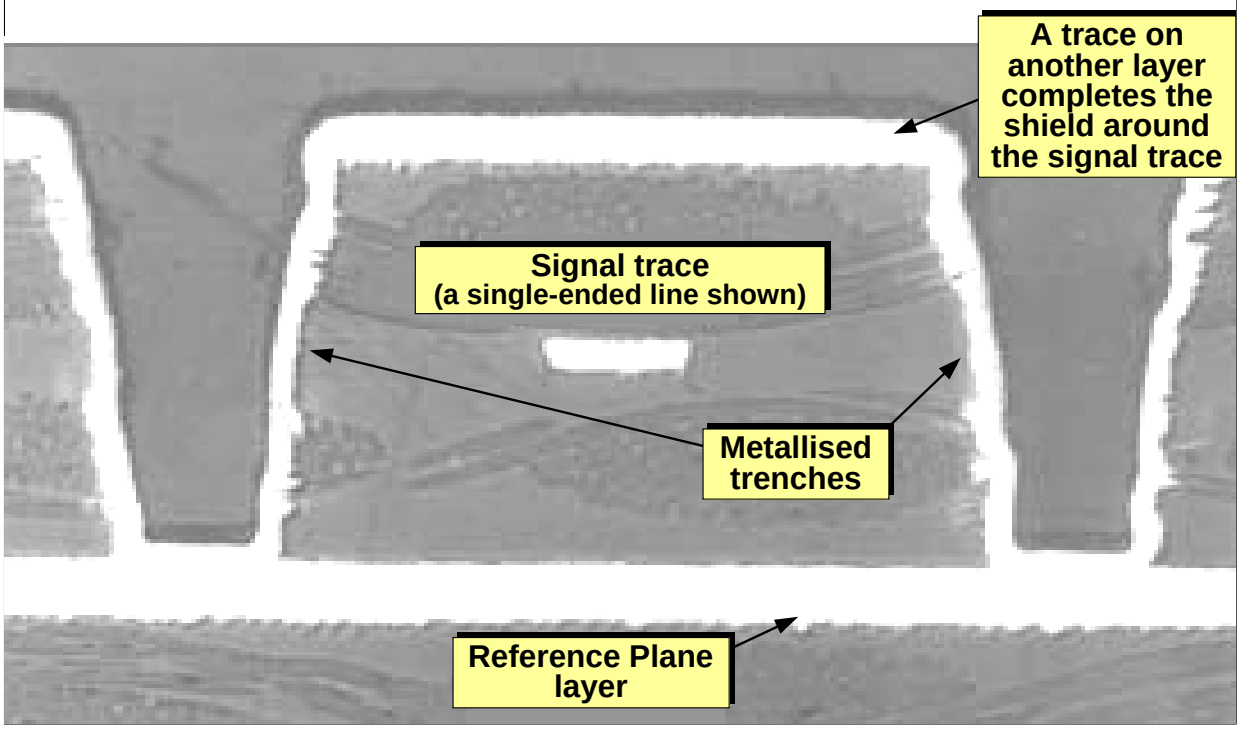


Figure 10

This is a real photograph of a PCB made with internal shielding for some of its traces, taken from [16].

Only a single trace has been shielded in this example, but the technique can just as easily be applied to differential pairs.

Filtering

- **It may be possible to low-pass filter some/all of the signals…**
  - ➔ **so that their imbalances would cause less of an impact on EMC (emissions and immunity)**
- **The rise/fall times of the filtered signals would need to be longer than the differential skew**
  - ◆ **the longer the better**
- **But only use filter capacitors in conjunction with series impedances (resistors or ferrites)**

Where the fastest rise/fall times or highest data rates or frequencies are not *really* required, it is usually possible to use low-pass filtering on the signals or noises – slowing down their transitions and/or reducing their highest frequencies. It might be practical to filter a driver output so much that transmission line techniques are not required at all, even for good EMC. This is a common technique for 'static' digital lines such as resets.

Where differential transmission line techniques are used, the aim of filtering is to make the rise/fall times of the signals so long that the effects of the imbalances are diminished. For example, the rise/fall times will probably need to be longer than the total differential skew created by all of the issues discussed in previous slides. In the case of waveshape imbalances, the aim would be to filter out the frequencies at which the imbalances are greatest. In general – the lower the -3dB frequency of the low-pass filter, the less will be the impact of imbalances on emissions and immunity. Sufficient filtering may not be achievable where data rates or signal frequencies must be very high.

Capacitors should not be used alone as signal filters. Observing a trace's voltage waveform with an oscilloscope will show that adding a capacitor at a device pin will slow down its rise/fall times and/or reduce its high frequency content. But what the oscilloscope does not show is that this capacitor increases the transient currents output by the driver, which increases the emissions of magnetic fields. These currents also tend to increase the voltage noise between planes, and so increase the emissions of electric fields from the plane edges.

Because of this, filter capacitors should always be used with series resistors or ferrites (as Tee, RC or CR filters) to limit any increase in transient current caused by the addition of the capacitors. The impedances of the series resistors or ferrites should be chosen taking the Z_0 of the line into account.

Where the imbalance and/or CM return path is poor, CM chokes can be used to raise the CM impedance – reducing the CM currents, and so reducing emissions and increasing immunity. These chokes can be quite large and are not low-cost, so it is best to design so that they are not required. They are more likely to be needed at the point where a differential line connects to an unshielded cable (e.g. UTP).

Using field solvers

- **PCBs can require many prototype–redesign iterations ('respins')**
- **Field solvers can reduce timescales and costs…**
  - ➔ **by designing differential pair routes for good balance *before* making the first prototype**
- **If field solver data can be included in circuit simulations…**
  - ➔ **analysis can include driver imbalances, for the best confidence in the first prototype PCB**

The previous slides have described the major causes of imbalance and their effects, and also briefly described some techniques for dealing with them, or at least reducing their severity.

Following all the EMC guidance in [1] will help control imbalance due to the PCB's structure. But real designs are always a compromise, and there are many complex issues to trade-off against each other.

To help reduce the number of prototype PCB manufacturing iterations ('respins'), to save time and cost overall and get to market quicker, it is recommended to use a field solver [1] to help design the PCB better at the start.

Field solvers allow many more possibilities to be explored much more quickly than is possible by building and testing prototype PCBs, and can be very cost-effective.

Field solvers will help design the differential pair routing for good balance, before making the first prototype.

But field solvers can't deal with everything: some design rules will also need to be adopted, such as using angled traces to compensate for woven dielectrics or phototool resolution. And 'test traces' [9] and the test instruments for testing them [10] at the 'Goods Receiving' department, will also be required for quality control of PCB manufacturers.

If combined with a circuit simulator that is able to import the simulation data from the field solver and include it in the functional simulation – the imbalance characteristics of the drivers and receivers can also be taken into account. This can achieve much better confidence in the good EMC and SI performance of the first prototype PCB.

Avoiding imbalance in differential transmission lines on PCBs

the end

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References, and further reading

The reference numbers are from the PowerPoint notes associated with this presentation

[1] ***Advanced PCB Design and Layout for EMC, Part 6 – Transmission Lines*****,**
Keith Armstrong, EMC & Compliance Journal, March, May and July 2005,
http://www.compliance-club.com/keith_armstrong.asp

[2] ***PCI Express Verification*****,**
Randy Weber, Printed Circuit Design & Manufacture, October 2004, pp 32-35,
http://pcdandm.com/pcdmag/mag/past_index.shtml

[3] ***Routing Differential Pairs,***
Denis Nagle, Printed Circuit Design & Manufacture, August 2003, pp 28-30,
http://pcdandm.com/pcdmag/mag/past_index.shtml

[4] ***Differential Signals Routing Requirements,***
Dr Abe Riazi, Printed Circuit Design & Manufacture, February 2004,
http://pcdandm.com/pcdmag/mag/past_index.shtml

[6] ***Avoiding Differential Pair Routing Violations*****,**
Dr Abe Riazi, Printed Circuit Design & Manufacture, August 2004, pp 26-29,
http://pcdandm.com/pcdmag/mag/past_index.shtml

References, and further reading continued…

[5] ***Common Mode Analysis of Skew*****,**
Howard Johnson: http://www.sigcon.com/pubsAlpha.htm

[7] ***Registration Techniques for Advanced Technology PCBs. (Or, so you think you can really do two-track routing?),***
Michael Barbetta and Joe Dickson, Printed Circuit Design & Manufacture, December 2004, pp 38-42, http://pcdandm.com/pcdmag/mag/past_index.shtml

[8] ***Advanced PCB Design and Layout for EMC – Part 4: Reference Planes for 0V and Power,***
Keith Armstrong, EMC & Compliance Journal, July 2004, pp 34- 43, http://www.compliance-club.com/keith_armstrong.asp

[9] ***Printed Circuit Board (PCB) Test Methodology, Revision 1.6 January 2000*****,**
Intel Corporation, www.intel.com/design/chipsets/applnots/29817901.pdf

[10] Polar Instruments,
http://www.polarinstruments.com/support/cits/cits_index.html

References, and further reading continued…

[11] ***Woven Glass Reinforcement Patterns,***
Gary Brist, Bryce Horine and Gary Long, Printed Circuit Design & Manufacture, November 2004, pp 28-33, http://pcdandm.com/pcdmag/mag/past_index.shtml

[12] ***The Impact of PCB Laminate Weave on the Electrical Performance of Differential Signaling at Multi-Gigabit Data Rates,***
Scott McMorrow and Chris Heard, DesignCon 05, January 2005, http://www.teradyne.com/prods/tcs/resource_center/whitepapers.html

[13] ***Still Good Bang for the Buck,***
Eric Bogatin, Printed Circuit Design & Manufacture, February 2005, page 54, http://pcdandm.com/pcdmag/mag/past_index.shtml

[14] ***Gigabit Backplane Design, Simulation and Measurement – the Unabridged Story,***
Dr Edward Sayre et al, DesignCon2001, available along with many other relevant papers from: http://www.national.com/appinfo/lvds/archives.html

[15] ***Robust Electronic Design Reference Book, Volume 1,***
John R Barnes, Kluwer Academic Publishers 2004, ISBN: 1-4020-7737-8

References, and further reading continued…

[16] ***Micro-Machining of Trenches to Form Shielded Transmission Lines,*** **Joan Tourne, Printed Circuit Design & Manufacture, April 2004, pp 34-37, http://pcdandm.com/pcdmag/mag/past_index.shtml**

[17] ***Schwarz-Christoffel Modelling of Shielded Tracks on a PCB*****, A Kapora and APJ van Duerson, Euro-EMC 04 Symposium, Eindhoven, Sep 6-10 2004, ISBN: 90-6144-990-1, pp 434-437**

High Speed Digital Design, a Handbook of Black Magic**, Howard W Johnson and M Graham, Prentice Hall, 1993, ISBN 0-1339-5724-1**

High Speed Signal Propagation: Advanced Black Magic**, Howard W. Johnson, Prentice Hall, 2003, ISBN 0-1308-4408-X**

EMC and the Printed Circuit Board, Design, Theory, and Layout Made Simple**, Mark I. Montrose, IEEE Press, 1999, ISBN 0-7803-4703-X**

Printed Circuit Board Design Techniques for EMC Compliance, Second Edition**, Mark I. Montrose, IEEE Press, 2000, ISBN 0-7803-5376-5**