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Guest Article - EFT/B Immunity

Helping you solve your EMC problems

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Analysis and prediction of EFT/B immunity

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Introduction

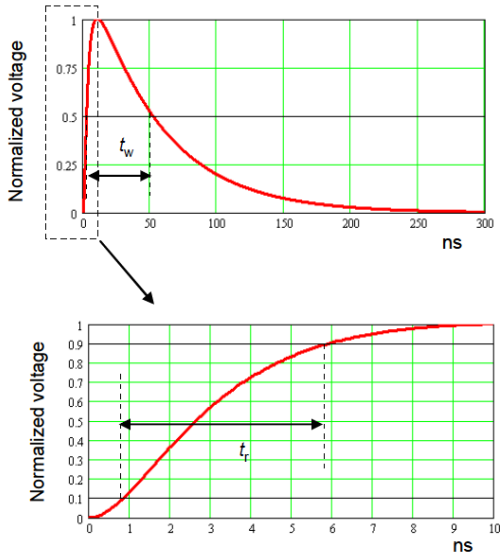
The EFT/Burst test of IEC 61000-4-4 is very common, called up as it is by most if not all EMC product immunity standards. It's a good test of the susceptibility of a product to switching transients on the mains and other interfaces. Perhaps because of this, it is often found to provoke susceptibilities, particularly in digital equipment, which can be hard to fix. A typical reason for this difficulty is that the waveforms of, and the actual coupling paths followed by, the transient disturbances may not be at all obvious. This article attempts to show how you might analyse such paths, and offers some measurement results on a simple circuit which illustrate the analysis.

EFT/B experiment

If the parasitic electrical properties of the mechanical structures can be understood, it is possible to derive an equivalent circuit for an assembly that is subject to the EFT/B stress and to simulate this in Spice. In fact, the operational circuit itself is mostly irrelevant as far as the coupling is concerned. The following demonstrates this approach.

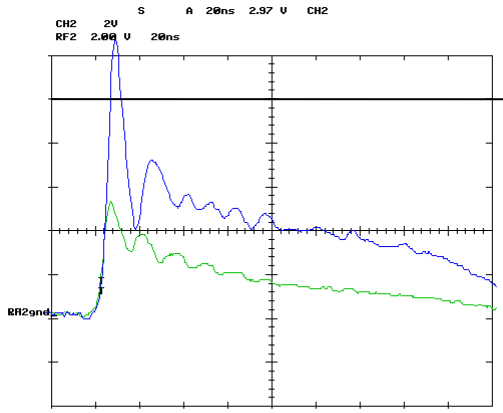
First, check the waveform of the generator

Before attempting to simulate the rest of the setup, it's a good idea to confirm the output waveform of the generator that is going to be used in the experiments. The idealized waveform of a single pulse in the burst, which will be used throughout this paper, according to IEC 61000-4-4 is as shown:



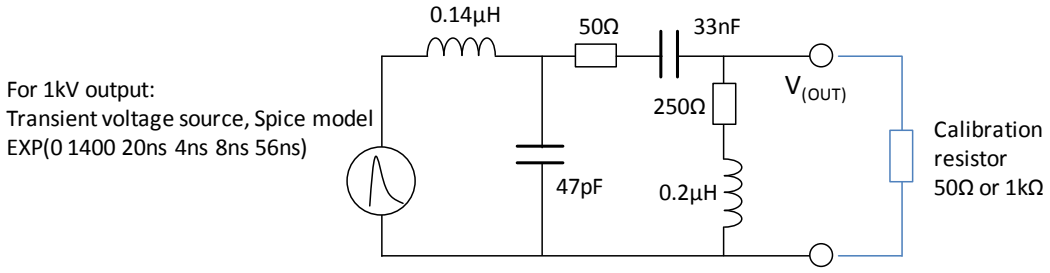
Tolerances:
rise time t_r = (5 ± 1,5) ns
Into 50 ohms:
pulse width t_w = (50 ± 15) ns
peak voltage, half indicated level ±10 %
Into 1000 ohms:
pulse width t_w = 50 ns, tolerance –15 ns to +100 ns
peak voltage, 0.95 indicated level ± 20 %

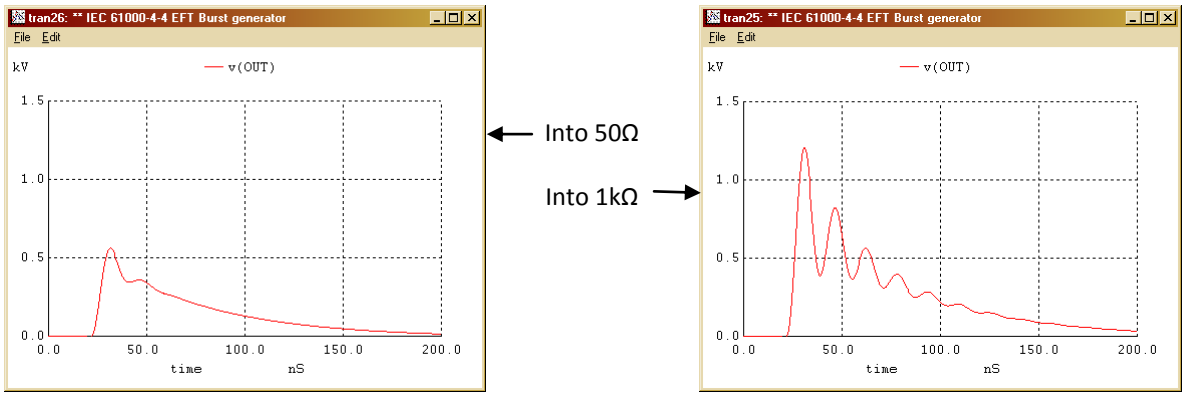
But the generator used by this author, a venerable Schaffner NSG1025, doesn't produce anything like this clean-looking waveform. Here's what it really looks like at 1kV indicated peak, into 50 ohms and into 1000 ohms. The generator has a coupling/decoupling network (CDN) for the mains supply coupling, whose earth (E) terminal is used throughout.



NB throughout this document, actual oscilloscope plots are presented as seen opposite, while the results of Spice models are shown in brown-framed screen captures

This requires a Spice model for the generator output which has some parasitic components to account for the evident ringing. The CDN-coupled source is modelled as shown, with results as below:





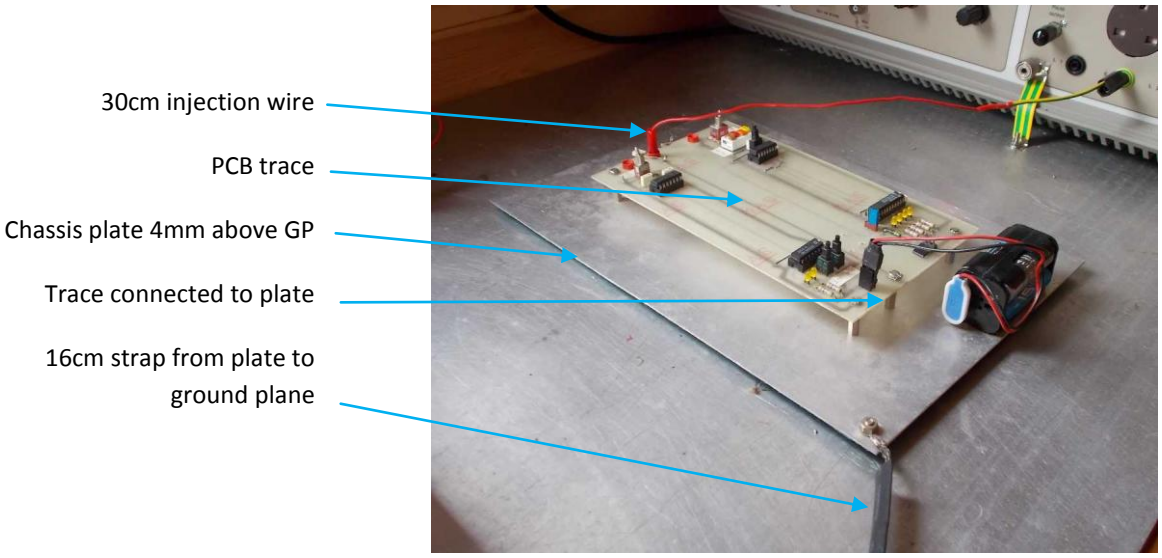
While not modelling the detail of the downstream waveform it does account for the initial rise and its amplitude. Incidentally, this model demonstrates why the later versions of the standard require a calibration both into 50Ω and into 1kΩ. A generator which doesn't meet the 1kΩ requirement, even

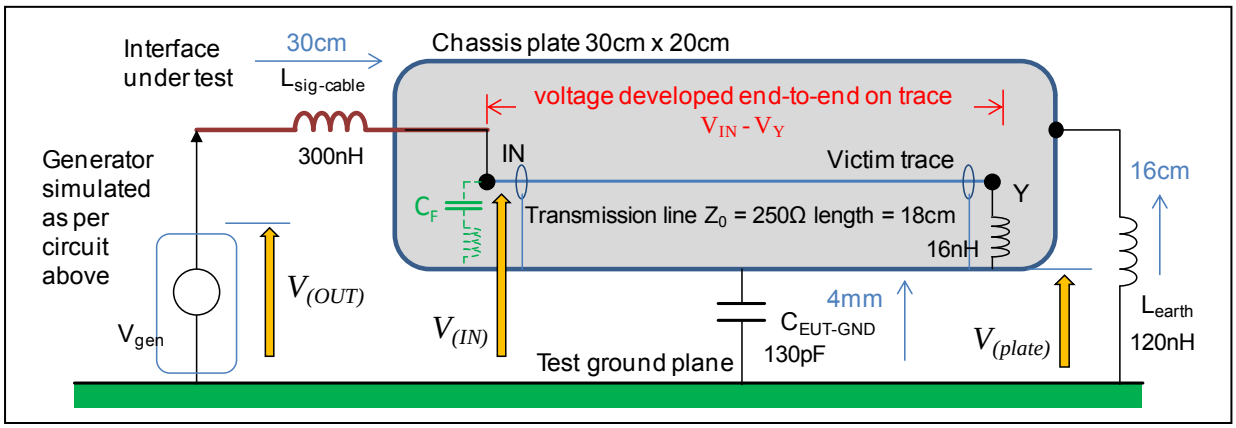
if it meets the early version of the standard which only required a 50Ω calibration, could overstress an EUT that offered a high impedance because of the excessive ringing when it is lightly loaded.

Analyse the EUT

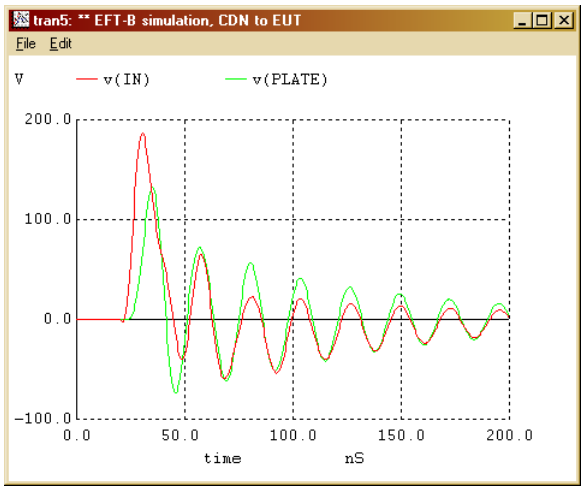
The experimental apparatus – highly simplified from a real product, of course – consists of a PCB carrying edge-triggered logic circuits that are normally static but which, when stressed with an EFT/B, will change state above a certain threshold. There is a separate "victim" trace alongside the circuits. The PCB is carried on a metal chassis plate to which the victim trace is grounded at one end, through a mounting pillar. This trace on the PCB is simulated by a transmission line against the plate, whose parameters represent its geometry. At the other end of the trace the EFT/B is fed in from the equivalent generator output, simulating a connected supply cable being tested via a CDN. The wire feeding it is 30cm long; the plate is grounded to the test ground plane via a 16cm strap and for the first trials the plate is positioned 4mm above the ground plane (this is not representative of the true test, where the separation is 10cm, but it illustrates the analysis better) which creates a calculated capacitance between the two of 130pF. This close proximity allows the plate to be treated as a lumped capacitance rather than a transmission line – see later.

A photograph of this setup and its equivalent circuit for the model are shown below.

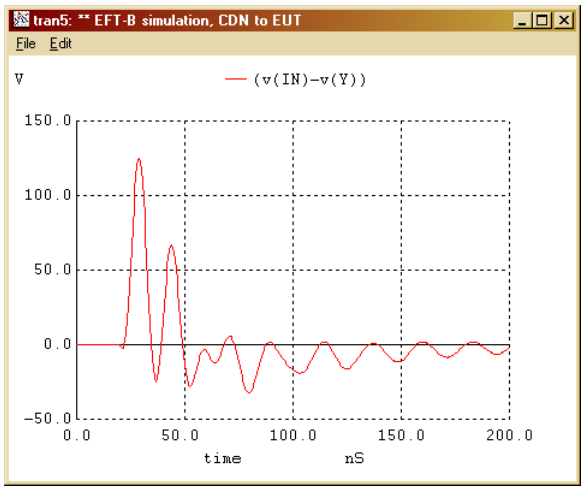




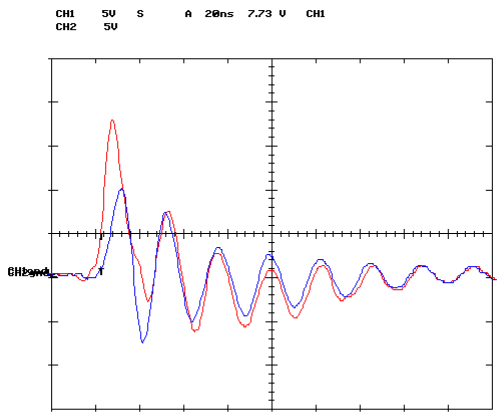
The voltages simulated under Spice at V_{IN}, V_{plate} and (V_{IN}-V_Y), for 500V in, are shown below. The colours correspond, with green in the model equivalent to blue on the oscilloscope plots.



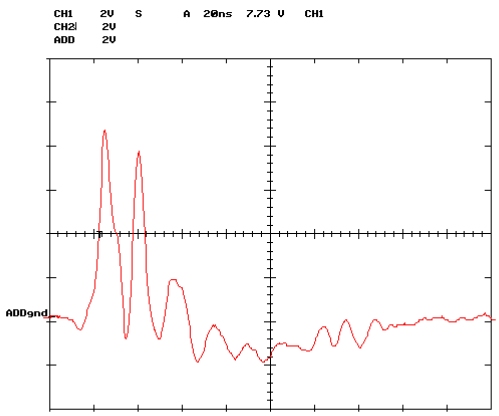
V_{IN}, Vplate



$V_{IN} - V_Y$



(50V/div)



(20V/div)

And the actual V_{IN} and V_{plate} and ($V_{IN} - V_Y$) are as above. Although the model shows a rather larger peak voltage than actually measured, the basic shapes of the waveforms as predicted by the model are very similar.

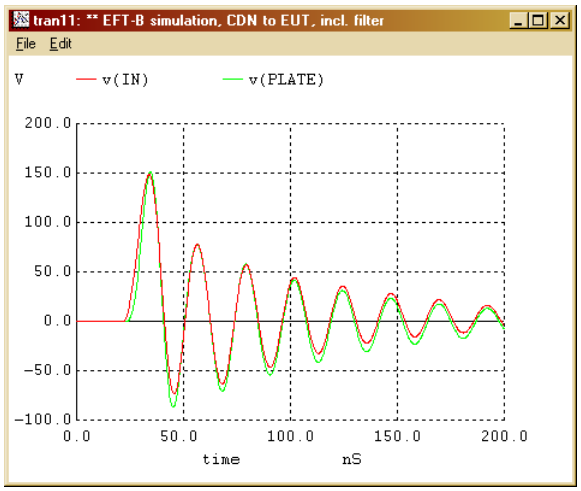
Notice the following features:

- Neither the input voltage nor the plate voltage are anywhere near the open circuit stress level of 500V;
- Substantial ringing on the plate at around 50MHz due to its capacitance and the grounding inductance;
- A peak of around 100V end-to-end along the victim trace.

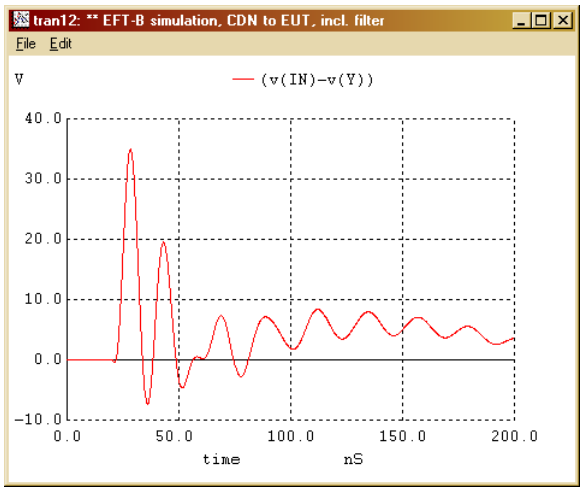
Further experiments show the effect of applying filtering on the input to the circuit 0V, and of reducing the capacitance between the plate and the ground plane.

Filtering

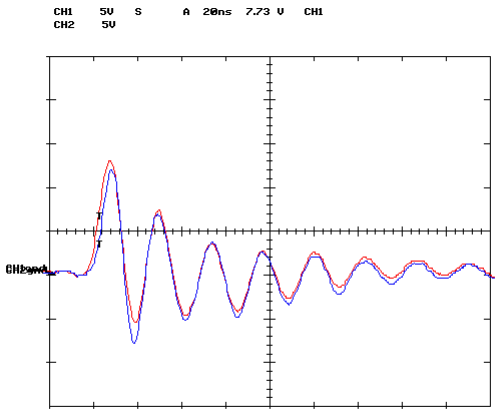
Now have a look at the effect of adding a filter capacitor C_F of 33nF plus parasitic inductance of 49nH between the input to the PCB and the chassis plate. (The total parasitic inductance can be deduced from a measurement of the component's self-resonance frequency, and adding the inductance of the connection to the plate.) The voltage end-to-end of the trace according to the model is much less, although not zero, and this is confirmed by the measurement:



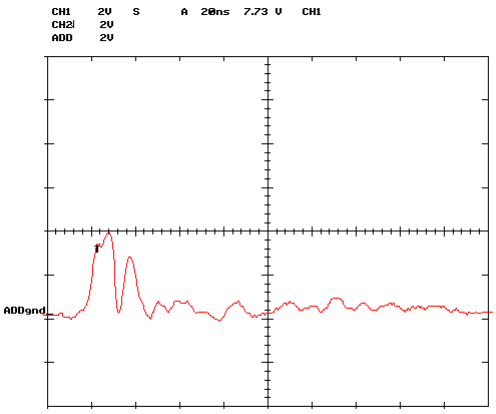
V_{IN}, Vplate



$V_{IN} - V_Y$



(50V/div)



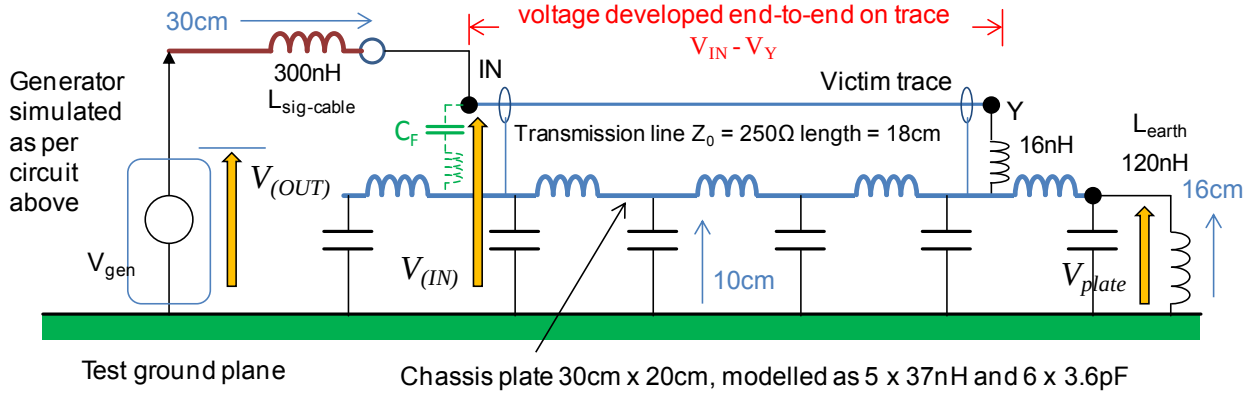
(20V/div)

Because of the capacitor's parasitic inductance the initial spike is still significant. It turns out from experimenting with the model that this parameter is the important one, not the capacitor's value; another interpretation of this is that the ringing frequency of about 50MHz is way above the component's self-resonance of about 5MHz.

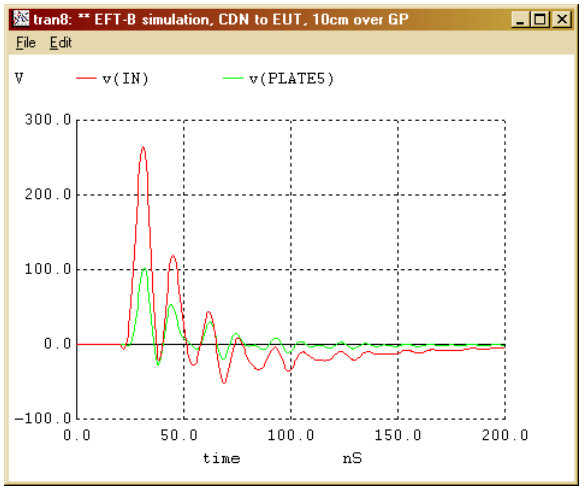
EUT capacitance to ground plane

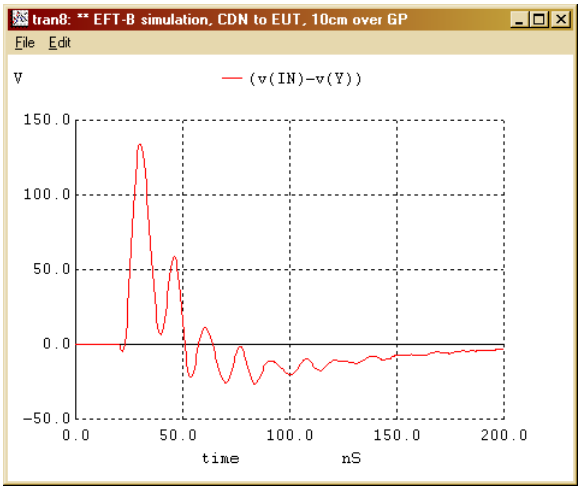
The above analysis is based on a separation between the EUT and the test ground plane of just 4mm, which is not typical of the standard test, but illustrates the effect the EUT-to-test-ground plane capacitance has on the ringing frequency, which is a function of the resonance between this capacitance and the inductance of the ground strap. Raising the height to the standard level of 10cm (on a polystyrene block) gives a calculated capacitance of 22pF, but the inductance of the chassis-to-

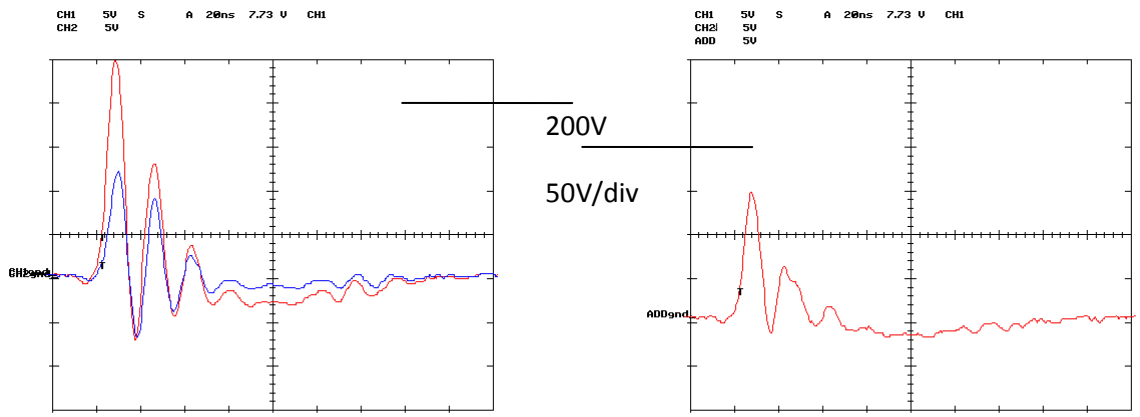
ground plane structure cannot now be ignored, and it is necessary to model this structure as a parallel plate transmission line in its own right. For the dimensions of 30cm long, 20cm wide, and 10cm high on polystyrene of ε_r = 2.6, the transmission line Z_0 is 93.5Ω. To properly model the physical arrangement of the PCB trace, the chassis plate and the ground plane, the chassis plate is divided into five 6cm lengths modelled by LC elements, so that the new equivalent circuit is as shown below.



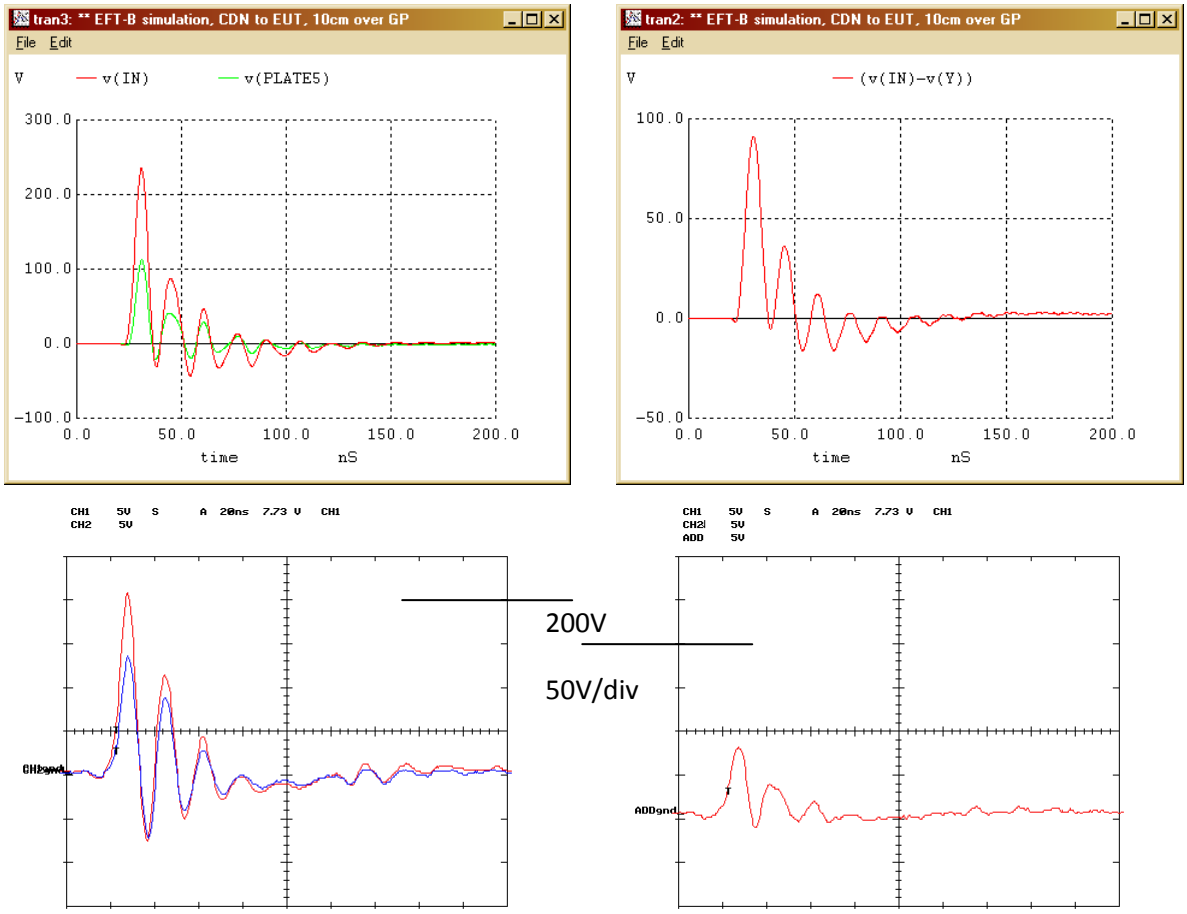
The results are as follows:







This shows again, good agreement between the model and the actuality. It clearly shows the ringing waveform at a higher frequency that exists on the whole chassis plate, and that a proportion of this waveform is coupled into the circuit. Adding a 33nF + 49nH filter capacitor at the node IN with respect to the chassis, as before, shows:



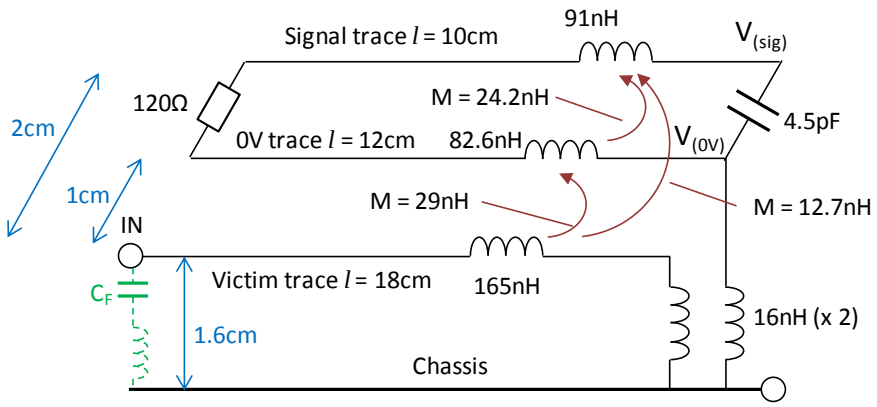
Again a reduction in the injected pulse, but limited by the capacitor's parasitic inductance, and apparently also by the increased impedance (because of the separation between the chassis and the test ground plane) along the chassis plate itself.

Coupled circuit response

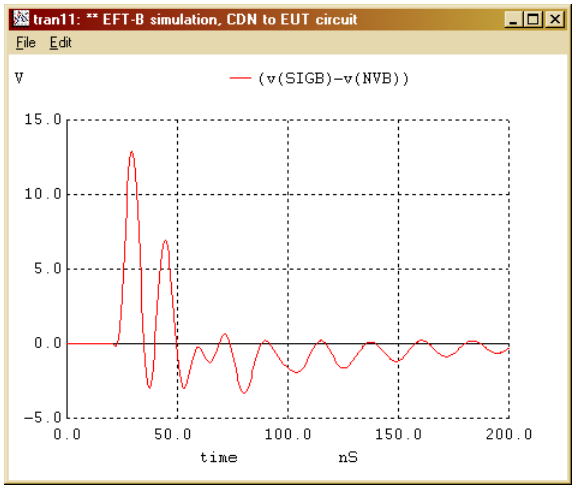
The waveforms denoted by (V(IN)-V(Y)) above refer to a single 18cm long track, with the burst injected at one end as if from a connector interface, and the other end grounded to the chassis, but with no actual circuit components connected. But there is a circuit which is located adjacent to this energised track, and it does get affected by the burst, even though it has no direct connection to it. The effect must be due to the mutual coupling between the victim and circuit tracks. Can this be modelled as well?

The circuit consists of a 74HC14 driver, with an assumed output impedance of 120Ω, feeding the clock input of a 74AC74 D-type flip-flop with an assumed input capacitance of 4.5pF, with a 10cm length of track from one to the other, separated from its 0V rail by 1cm, and with the 0V rail separated from the source track by another 1cm; this means the signal track is 2cm away from the source track.

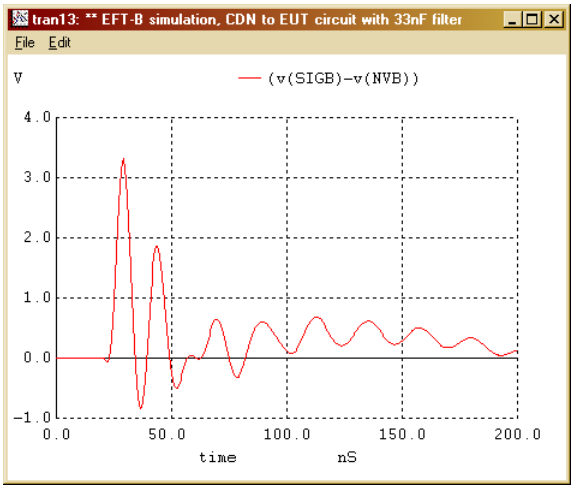
The effective equivalent circuit looks like this:



This circuit takes account of the mutual inductive coupling between the principal source and victim tracks. This can be embedded in the previous Spice circuit for a separation distance from the test ground plane of 4mm. Then the induced signal of interest is that which appears across the 4.5pF input of the 74AC74, as this will potentially cause the device to change state. This is what it looks like from the model, at an applied stress of +500V, without and with the same 33nF + 49nH filter capacitor C_F at the IN node to chassis:



No filter



33nF filter capacitor (NB 4V:15V scale difference)

Unfiltered, a peak of about 13V appears at the D-type's input – no account is taken in this model of the clamping protection diodes in the actual device. In addition, the model as shown has not considered the capacitive coupling which also exists between the tracks; however, when an approximately calculated capacitance (0.75 – 1.1pF) is introduced between the source and victim tracks at each end, there is virtually no change in the resultant waveform, suggesting that inductive coupling is dominant.

With the filter capacitor added, the peak amplitude of the induced voltage has dropped to around 3V, about a quarter of the unfiltered value. This correlates reasonably well with the observed susceptibility of the circuit, whose trip threshold depends both on the polarity of the pulse and whether the clock input is held statically high or low; the device is sensitive to positive-going clock

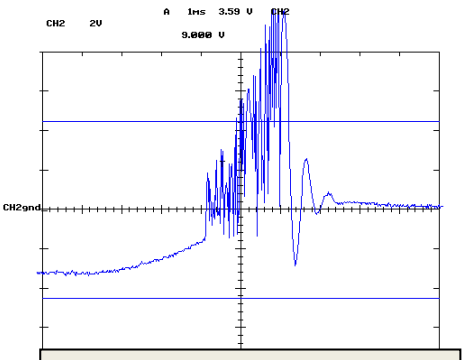
edges. Without the filter and the clock held high, the device is immediately susceptible to the lowest level (around 300V) of *negative* going pulse; with clock held low, it is immediately susceptible to the lowest level of *positive* going pulse. With the filter, the threshold rises to between 1.4 and 2.1kV depending on the polarities.

Coincidence and timing issues

The discussion so far has looked only at how the EFT/B pulses can travel across and through a product and can then disrupt its operation at susceptible circuit nodes, if the induced pulse amplitude is high enough. But there is another aspect to whether the circuit operation is actually disrupted, and that is whether the pulses coincide with a susceptible *time slot*. In a digital system, it's usually the case that the operation is most susceptible during a transition, either of a clock signal or an edge-triggered input; outside these transition points, a higher level is needed to cause corruption. And, as above, different quiescent states will have different susceptibility levels.

In the test, each burst consists of 75 short pulses, repeated either at a 5kHz rate (most legacy standards) or 100kHz rate (newer requirement). This burst duration of either 15ms or 0.75ms is then repeated every 300ms for a minute in each polarity. So there are approximately 15000 pulses in each polarity which, assuming the application is asynchronous, will give a high probability of coincidence with a susceptible transition time.

But this standardized pulse definition doesn't represent typical transient occurences in the real environment. Such pulses don't come along at a regular 300ms interval for a minute, and don't have a defined 5kHz or 100kHz repetition rate. For interest, a typically aggressive switching transient, recorded on the supply to a mains-powered solenoid as it was switched off by a relay, looks like the graph opposite.



1ms/div, 900V between blue lines

The standardized EFT/B test, then, can artificially over-stress a product in some circumstances:

- If it is designed to cope with and/or recover from corruption that occurs occasionally, but is defeated by a consistent 300ms periodicity;
- If it has a particularly sensitive analogue signal bandwidth, or digital repetition period, centred on 5kHz or 100kHz;
- If it has a communication protocol that can recover from occasional lost packets, but again can't cope with repeated bursts of 5kHz or 100kHz every 300ms.

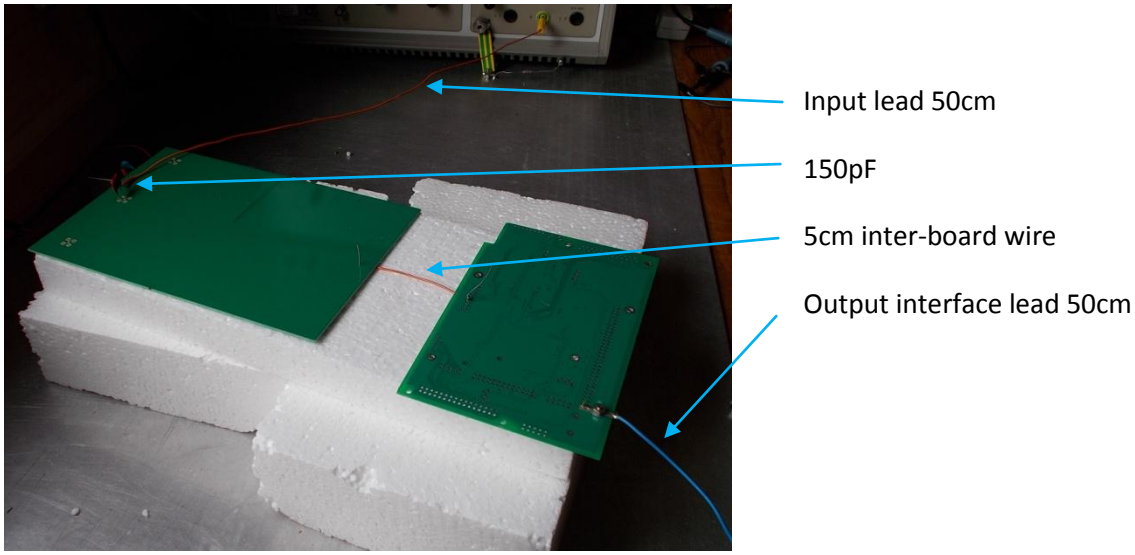
In each of these cases, the IEC 61000-4-4 test can fail a product which could be adequately immune in its real environment.

Another product design

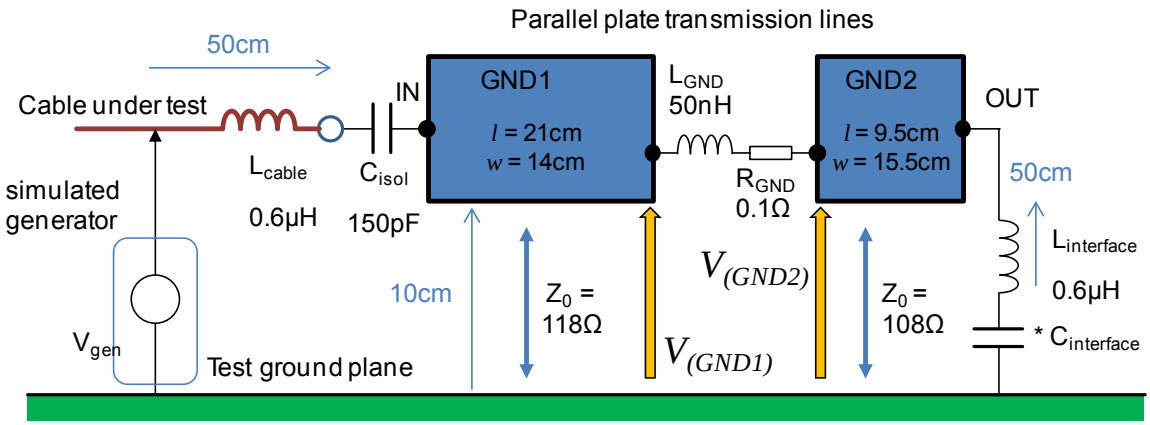
The presentation so far has shown that modelling a simple geometry with a PCB on a chassis over a ground plane produces tolerably valid results. What happens with a different two-PCB assembly with no chassis?

What we will do here is look at the difference due to the pulse in the voltage appearing between two ground planes on boards which are connected to each other by a 5cm length of wire. This voltage, it can be assumed, would be likely to interfere with communications between one board and the other, depending on the common mode rejection of the interface circuits. One board has the EFT/B pulse applied to it through a 50cm lead and 150pF at one end, simulating for instance the test to a mains input where the isolation capacitance across the PSU's switching transformer is 150pF. The other end of the other board can have a number of options: no connection at all, a grounded 50cm wire, or a 50cm wire with either a 22pF or 52pF capacitor to the ground plane, which will simulate different output interface conditions.

The test setup uses a couple of spare blank PCBs that were floating around the author's scrap box. The ground plane of the first one is continuous at 21 x 14cm, of the second one is somewhat broken at 9.5 x 15.5cm. The two boards are positioned 10cm above the test ground plane on expanded polystyrene blocks. A photograph is shown below.

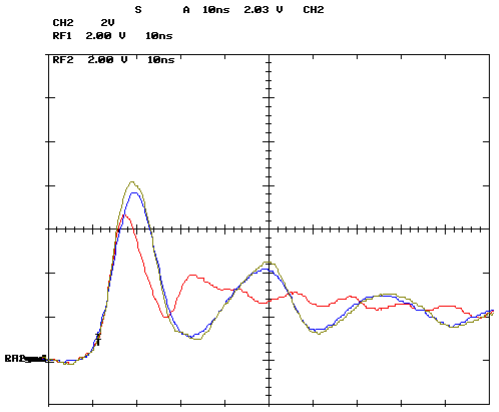


The equivalent circuit is shown below, with *$C_{interface}$ being one of open circuit, short circuit, 22pF or 52pF. The two boards' ground planes are modelled as parallel plate transmission lines with their parameters determined by dimensions and the ε_r of thepolystyrene block.



No OUT connection

The experimental setup is first tested at 500V without any load cable at the OUT node, i.e. with $L_{interface}$ and $C_{interface}$ missing. The measurements show, unsurprisingly, that there is little difference between the different nodes on the ground planes, although the effect of adding the ungrounded capacitance is to create a lower ringing frequency. The red trace shows the 500V 1kΩ calibrated waveform compared to the measured waveforms at IN and OUT.

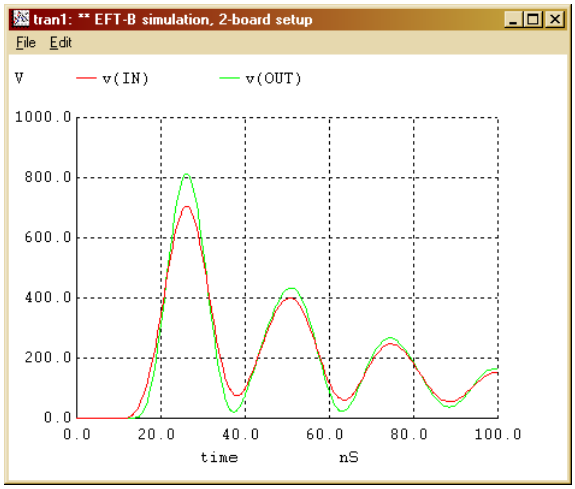


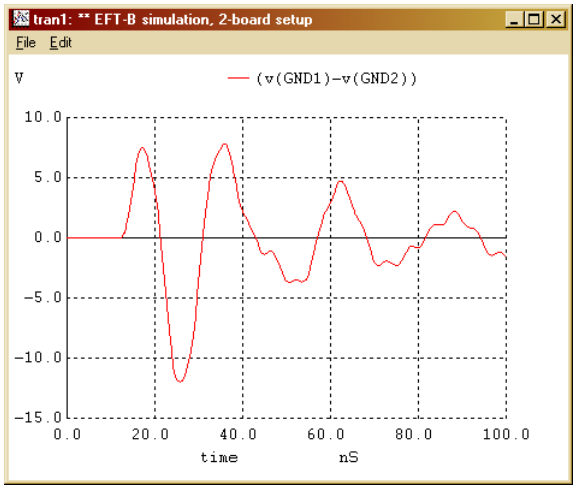
Red = 1kΩ calibrated waveform @ 500V

Blue = V(IN)

Brown = V(OUT)

200V/div, 10ns/div

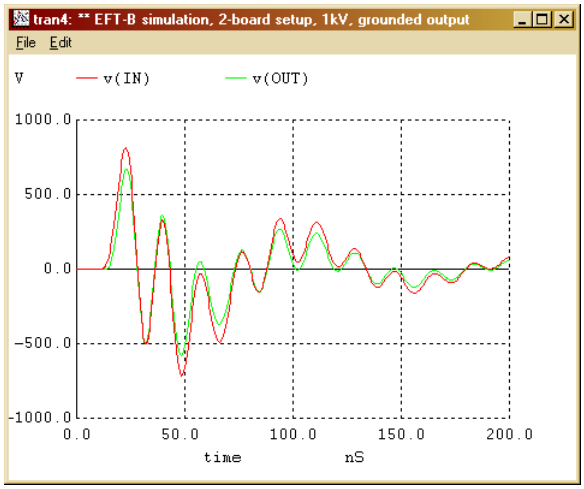


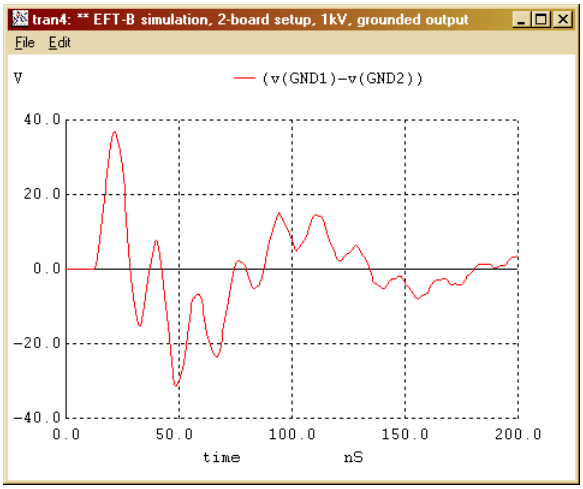


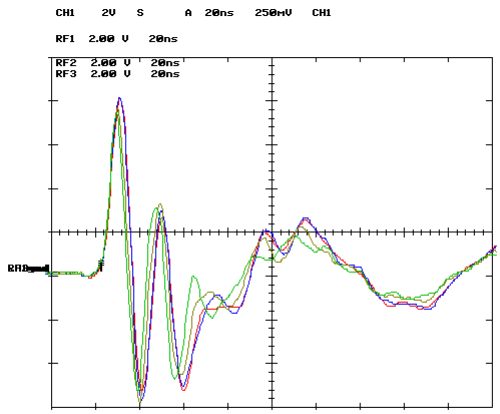
The model gives us a similar picture, with the ringing frequency increased as determined by the LC load presented by the boards and their connected wiring. It also shows, as in the measurement, that the voltage peak at the output end of the board pair is *greater* than that at the input. The peak *negative* voltage between the two boards, across the 50nH inductance of the connecting wire, is 12V for a +500V stress.

Connecting OUT to the test ground plane

Adding a grounded connection via a 50cm interface cable to the output completely changes the coupling. Current now passes out of the OUT node and therefore the series inductances give a greater voltage drop. These plots are set for a stress of 1kV and a total duration of 200ns.







Red = V(IN)

Blue = V(GND1)

Brown = V(GND2)

Green = V(OUT)

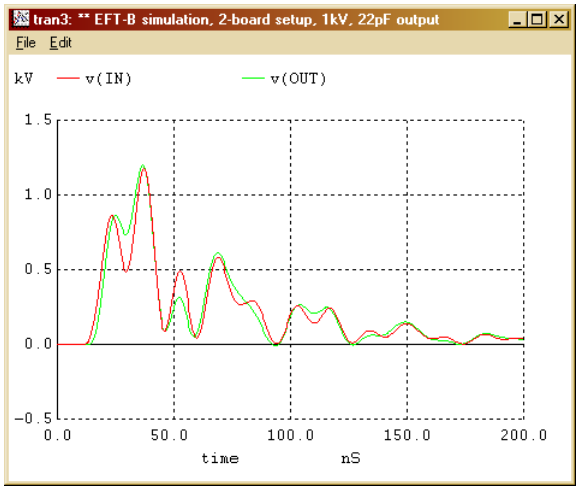
200V/div, 20ns/div

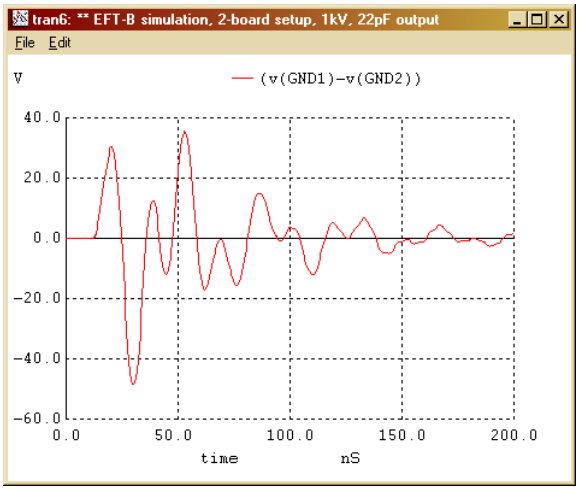
The voltage between the ground planes now has a first *positive* peak of nearly 40V and a following negative peak of 30V. These two peaks last for around 10-15ns each, easily enough to disrupt high-speed interboard signalling.

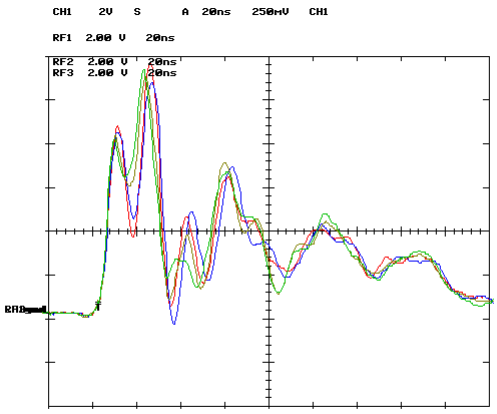
Adding a series capacitance to the connection

If the OUT interface is connected to an ungrounded ancillary apparatus, then we cannot say that the above situation is representative. Instead the far end of the 50cm interface cable is connected to the test ground plane via a small capacitor, which represents the self capacitance in common mode of the ancillary apparatus. In this example we have tried two different capacitor values, 22pF and 52pF. These could legitimately represent moderate-sized products at the regulation 10cm above the ground plane.

Here are the plots for 22pF, with the stress set to 1kV.







Red = V(IN)

Blue = V(GND1)

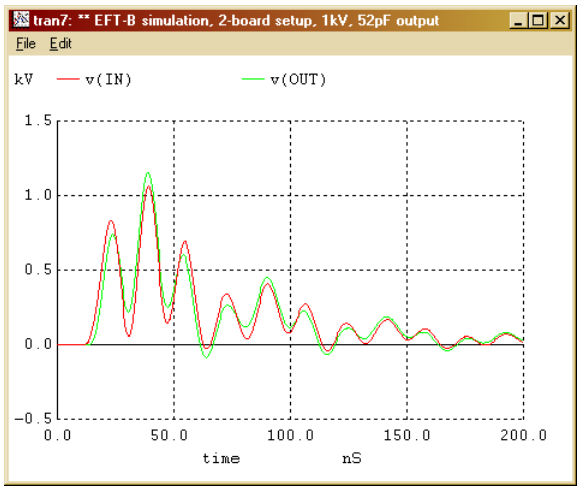
Brown = V(GND2)

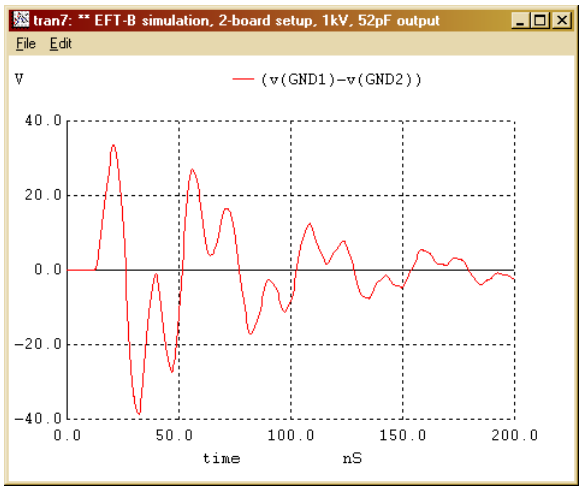
Green = V(OUT)

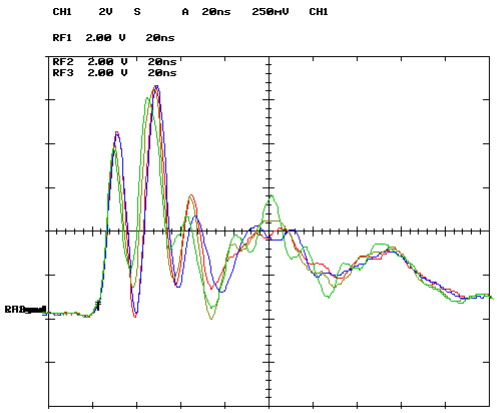
200V/div, 20ns/div

We still have peaks of 30 – 40V between the planes, although in the opposite polarity to before.

Finally, the same again but with a 52pF capacitor to ground at the end of the 50cm output wire.







Red = V(IN)

Blue = V(GND1)

Brown = V(GND2)

Green = V(OUT)

200V/div, 20ns/div

Not identical, but not greatly dissimilar to the 22pF case. Note that in all cases the early part of the transient is well modelled, even if the later part is less so.

Conclusions

There are a number of insights that can be drawn from the data presented here.

- Consider the electrical behaviour of mechanical components: you don't need to look at the circuit schematic, rather look at the structures and wires that are present in the product as components – inductors, capacitors, transmission lines and to a lesser extent resistors – in their own right, and draw up a schematic which shows their interconnections in the context of the external test setup
- Simplify this schematic as far as possible, but not too far[1]; understand where inductance dominates over capacitance or vice versa, and where both are important; be prepared to add loss components where necessary
- Modelling the appropriate circuit schematic can lead you very close to seeing the actual waveforms that are present at critical points in the structure

[1] Remember Einstein: "The supreme goal of all theory is to make the irreducible basic elements as simple and as few as possible without having to surrender the adequate representation of a single datum of experience."

- The model will also enable options to be evaluated for improving immunity to the test, such as adding filter components, as long as the parasitics of the components are included
- The actual waveforms and levels that are present in and through the EUT during an EFT/B test are nothing like the idealised waveforms presented by the generator: they are heavily modified by the parasitic impedances of the various coupling paths, including the connecting cables and the presence and proximity of the test ground plane, and consequently have a large and variable-frequency ringing component
- External interfaces other than the one being tested have a significant effect on the coupling, and must always be carefully considered and controlled in the test plan

Finally, the presence of the ringing, and the fact that it is principally a function of the resonances due to parasitic reactances of the constructional elements, suggests that a similar kind of analysis could be carried out in the frequency domain and result in pointers to susceptible frequencies that might appear in the IEC 61000-4-6 conducted immunity test. This is a subject for further experimentation.

Appendix: equations for calculating parasitics

Magnetic coupling

Self inductance of each conductor circuit, wire diameter d, height h over the ground plane

$$L_{cct} = 0.002 \cdot \ln\left(\frac{4h}{d}\right) \mu H/cm$$

Self inductance of short length of grounded conductor, length x cm

$$L_g = 0.002 \cdot x \cdot \ln\left[\left(\frac{4x}{d}\right) - 0.75\right] \mu H$$

Mutual inductance between conductors, separated by D cm

$$M = 0.001 \cdot \ln\left[1 + \left(\frac{2h}{D}\right)^2\right] \mu H/cm$$

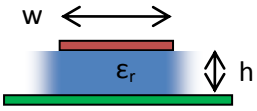
Coupling coefficient

$$K = \frac{M}{\sqrt{L_{cct1} \cdot L_{cct2}}} = 0.44$$

Transmission lines

Stripline over a ground plane, 0 < w/h < 10

$$C = 0.0885\varepsilon_r \left(\frac{w}{h}\right)\left\{1 + \left(\frac{h}{\pi w}\right)\left(1 + ln(2\pi w/h)\right)\right\} \; pF/cm$$



Wide strip (h/w < 5)

$$L = \mu_0\mu_r\left(\frac{h}{w}\right) \; H/m$$ (approx) ($\mu_0 = 4\pi \cdot 10^{-7}$)

Narrow strip (h/w > 5)

$$L = \left(\frac{\mu_0\mu_r}{2\pi}\right)\cosh^{-1}\left(\frac{h}{2w}\right) \; H/m$$

$$Z_0 = \sqrt{\frac{L}{C}}$$ ohms

For parallel plates, C = 0.0885·(A/d) pF where A is overlapping area in cm^2, d is separation in cm; this works sufficiently well for w/h > 10