

Another EMC resource from EMC Standards

Analogue design techniques for S/N (SNR) and immunity to EMI



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Keith Armstrong CEng, FIET, Senior MIEEE, ACGI, EurIng(Gp1)
phone/fax: +44 (0)1785 660 247
keith.armstrong@cherryclough.com
www.cherryclough.com www.emcstandards.co.uk



Good Electromagnetic (EM) Engineering...

- is cost-effective SI, PI and EMC engineering:
 well-proven to save time & money in all lifecycle stages,
 helping to increase profits & reduce financial risks...
- for PCBs, modules, sub-assemblies, devices, products, equipment, vehicles, sub-systems, systems, installations, etc., etc.; of <u>any</u> size, in <u>all</u> applications
- see Module 1 especially 1.15 (also in Webinar 1c) and 1.16 (also in Webinar 1d)
- This Module contains many EM Engineering guidelines that should also be used as an initial design checklist: any that can't or won't be followed identify a project risk! see Module 1, section 1.16 (also in Webinar 1d)
 - to adapt any λ -based design guidelines to different EMC standards, see Module 1, section 1.18 (also in Webinar 1d)



Contents

- Introduction: S/N, SNR and immunity to EMI
- System design techniques
- Circuit design techniques
 - Using a 'solid' 0V plane
 - Using circuit segregation
 - Improving linear bandwidth and stability
 - Improving recovery from saturation and clipping
 - Suppression of noise entering via the input(s)
 - Suppression of noise entering via the power rail(s)
 - Suppression of noise entering via the output(s)
 - Cabling and shielding techniques for noise suppression
- Hysteresis is needed for all comparators



Introduction: S/N, SNR and immunity to EMI



Introduction

- Good S/N ratio (or SNR) and good EMI immunity has always been a problem for analogue circuits...
 - especially if regulatory compliance requires immunity tests
- These techniques work on both 'internal EMC' and 'external EMC' (see later) to solve both problems quickly, with least cost...
 - so should be used even where EM immunity compliance is not a mandatory requirement...
 - to save time and money overall; reduce financial risks; increase competitiveness, and improve functional performance to please customers

emc8b v1.0

Electromagnetic Compatibility EMC

'External' EMC

The real world of 'External' EMC

EMC test lab measurements

'Internal' EMC S/N ratio Noise margin **Overshoot** Ringing **Eye closure** Signal integrity **Power integrity Crosstalk Clock jitter** Etc., etc..



An example of real-life benefits

- These design techniques mostly began as methods for improving SNR in mixed-technology products...
 - and were found to improve resistance to EMI, so recently have mostly been used for good EMC immunity design...
 - a highly-respected 30+ year UK maker of custom Pro-Audio analogue mixing desks started to use these design techniques when they began using microprocessors...
 - they found that even with one micro per channel their SNR was 10dB lower than their best-ever pure analogue desk...
 - testing/installation times were both cut by more than half...
 - they were able to improve their product spec and double sales on the same site with the same number of staff, with very many fewer complaints under warranty



The focus is on circuit design...

- but controlling analogue SNR and EMI problems also requires the use of other good EMC design techniques:
 - PCB design and layout Cabling Filtering etc...

Power decoupling
Shielding
ESD and surge protection

- and most products will also need the emissions and immunity of its digital, control, display and switch-mode power converter circuits dealing with too
- These are not described here (in any great detail)...
 - but they are comprehensively described in our other course modules, articles and textbooks