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EMC design of Switching Power Converters Part 7 (continued 4)

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EMC design of Switching Power Converters

Part 7 *(continued 3)* — Suppressing RF noise in DC inputs, outputs, and DC-Links

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Contents

Issues 93-100 of The EMC Journal carried the preceding parts of this "Stand Alone" series – my attempt to cover the entire field including DC/DC and AC/DC converters, DC/AC and AC/AC inverters, from milliwatts (mW) to tens of Megawatts (MW), covering *all* power converter applications, including: consumer, household, commercial, computer, telecommunication, radiocommunication, aerospace, automotive, marine, medical, military, industrial, power generation and distribution, in products, systems or installations.

Hybrid & electric automobiles, electric propulsion/traction; "green power" (e.g. LED lighting); and power converters for solar (PV), wind, deep-ocean thermal, tidal, etc., are also covered.

Issues 93-95 used a different Figure numbering scheme from the rest, for which I apologise.

I generally won't repeat material I have already published, instead providing appropriate references to the EMC Journal [14] and my recently-published books based on those articles [15], so that you don't get bored by repetition.

7 Suppressing RF emissions from inputs and outputs

I began Section 7 in Issue 98 [72] and so far it has continued up to Issue 100 [92]. Despite my aim to only publish 'stand-alone' articles, each covering a single topic, the issue of suppression is so large that it is impossible to publish it all in a single issue.

Suppression is such a large topic, because it is so difficult to do and requires attention to a great many details. It is also very costly.

Please don't forget that it is much better (more cost-effective, shorter time-to-market, see section 7.1 in [72], [11] and Chapter 1 of [5]) to design the power converters in such a way as to minimise their input and output emissions. These design topics were covered in the early parts of this series, [13] [42] [64] [65] and [66], because they are more important for technical and financial success.

7.6 Filtering DC with big capacitors

7.6.1 Introduction

The DC to be filtered that I will discuss here could be a DC power input, DC power output, or an intermediate DC power-coupling stage (generally called a DC-Link).

The example used in the previous issue on shielding power converters' AC output cables, was based on an AC-AC inverter powered by an AC supply, driving an AC motor.

Exactly the same noise emission issues apply to the AC inputs or outputs of AC-DC or DC-AC converters, as apply to their DC outputs or inputs considered in this article.

These noise emission issues also apply to the inputs and outputs of DC-DC converters. And any noise voltage on a converter's DC-Link tends to 'escape' via the converter's power inputs and outputs.

But the big advantage that we have when filtering DC inputs, outputs and DC-Links, is that we can use very large values of capacitance. Figures 7.6-1 and 7.6-2 show AC-DC and PWM AC-AC converters respectively, with simplified sketches of the noise voltages at various points in their circuits.

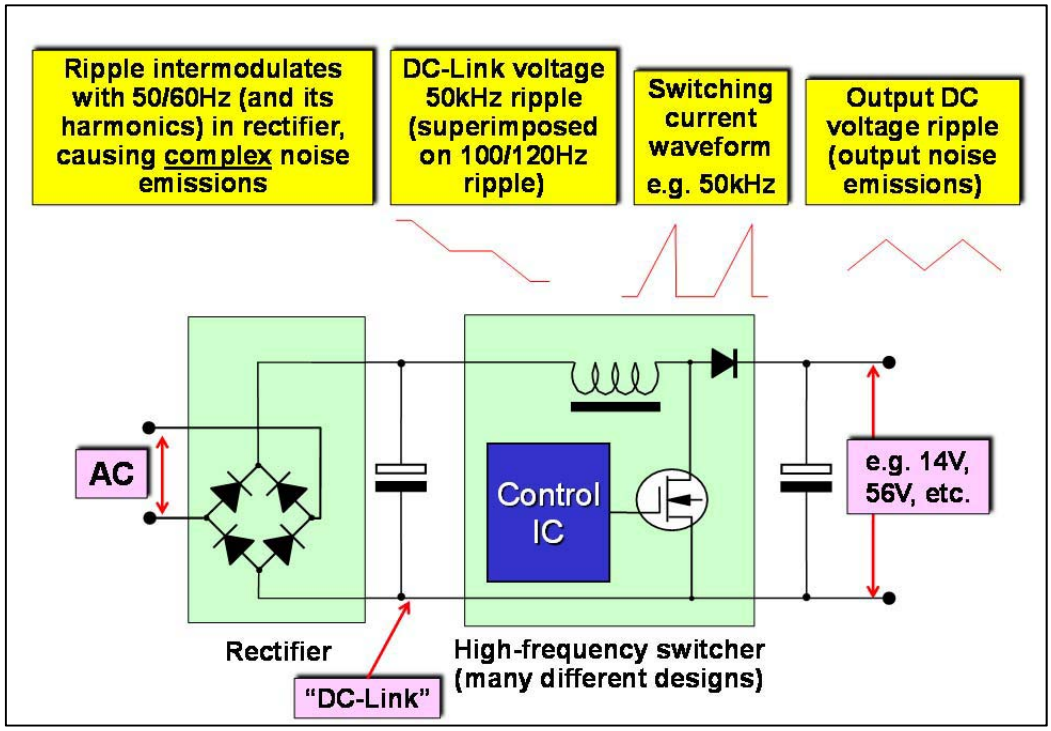


Figure 7.6-1 Example of the noise voltages in the circuit of a simple AC-DC converter

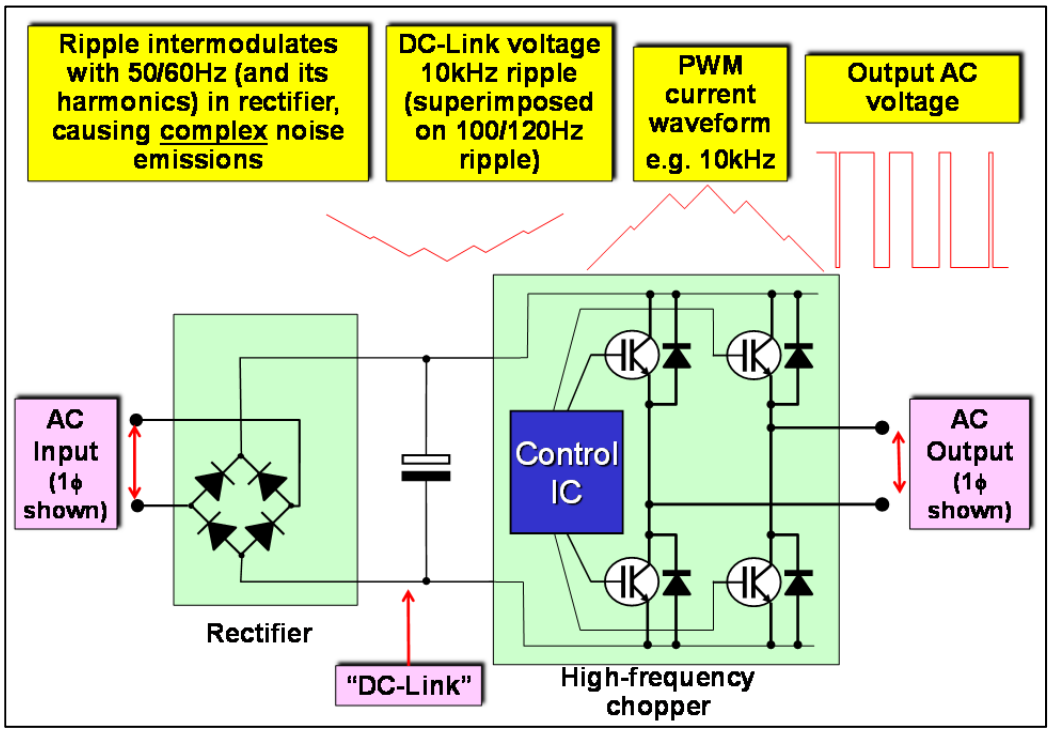


Figure 7.6-2 Example of the noise voltages in the circuit of a simple PWM inverter

Note that no noise waveform is drawn for their AC mains inputs – because these waveforms are too complex. The bridge rectifier acts as a frequency mixer, so that the rectified AC mains frequency and its harmonics intermodulates with the DC-Link's noise frequency and harmonics.

Figure 7.6-3 shows an example of the noise spectrum emitted from the 50Hz (designated f_1) mains power input of a 700kW variable-speed AC motor drive running at 39.4Hz (designated f_2), with the intermodulation products (IPs) marked.

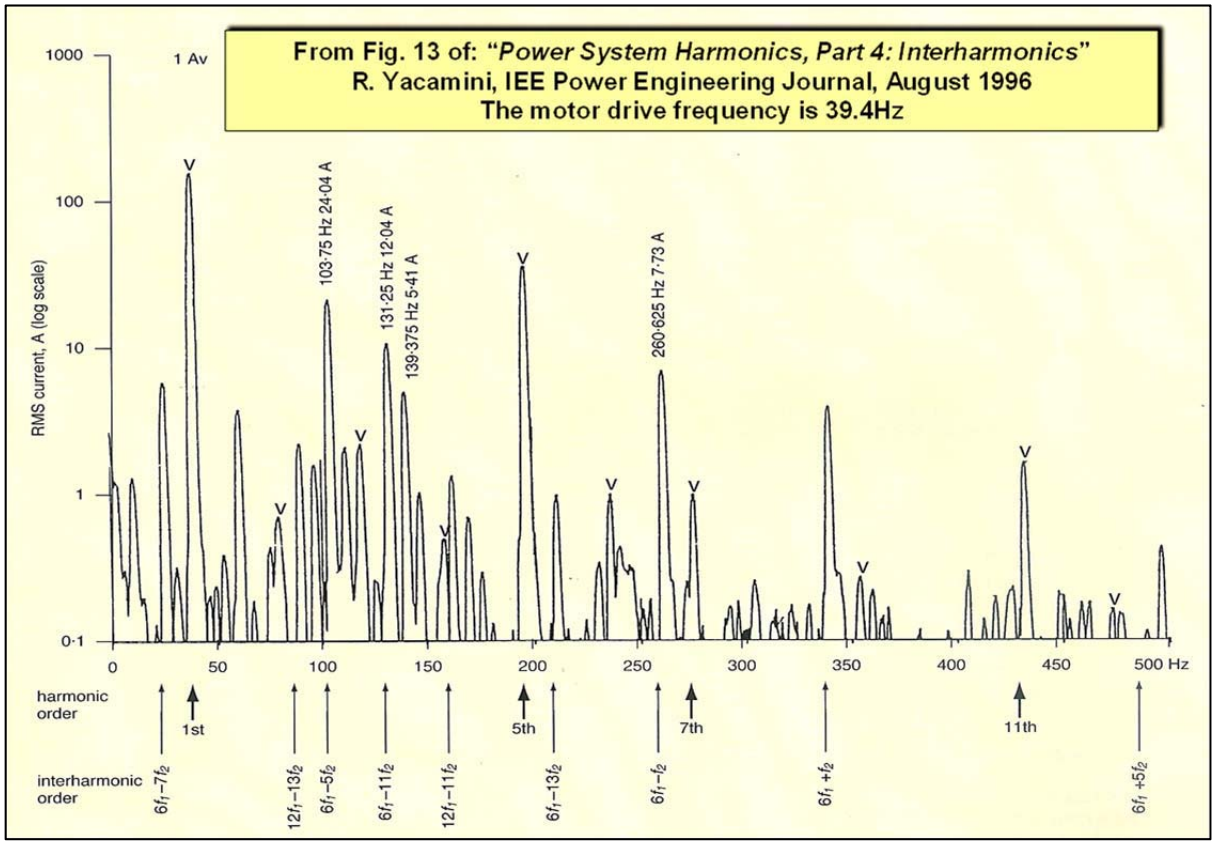


Figure 7.6-3 Mains input noise emissions (unfiltered) from a high-power AC motor drive

Thus we have:

- Approx. 6A rms of noise current at $6f_1$-$7f_2$ (i.e. 24.2Hz)
- 110A rms of noise current at f_2 (i.e. 39.4Hz)
- Approx. 3A rms of noise current at $12f_1$-$13f_2$ (i.e.87.8Hz)
- 24A rms of noise current at $6f_1$-$5f_2$ (i.e. 103Hz)
- 12A rms of noise current at $6f_1$-$11f_2$ (i.e. 133Hz)
- 5.4A rms of noise current at $24f_1$-$34f_2$ (i.e.140Hz)
- Approx 50A rms of noise current at $5f_2$ (i.e.197Hz)
- 7.73A rms of noise current at $6f_1$-f_2 (i.e.260.6Hz)
- Etc…

The harmonics of f_1 are all in multiples of 6, because a symmetrical 3-phase bridge rectifier – also known as a 6-pulse rectifier – has output ripple at the fundamental frequency of 300Hz (i.e. $6f_1$), plus 2nd, 3rd, 4th, etc. harmonics at 600Hz ($12f_1$), 900Hz ($18f_1$), 1200Hz ($24f_1$) etc.

The harmonics of f_2 start with the 5th, because symmetry in the 3-phase chopper circuit mostly cancels out the even-order harmonics and the triplens (3rd, 9th, 15th, etc.) leaving only the 5th, 7th, 11th, 13th, 17th, 19th, etc. at significant levels.

Then intermodulation between these two sets of harmonic currents flowing simultaneously in the non-linear the bridge rectifier causes all their various frequencies to be added and subtracted, generating hundreds more noise currents at brand-new frequencies, known as Intermodulation Products (IPs).

Chapter 7.3 of [4], which is the same as Chapter 2.9.3 of [5], discusses demodulation and intermodulation in general, but fails to give a good idea of the huge intermodulation complexity that results from having just two different frequencies in a circuit as simple as a single diode, the simplest possible situation, shown in Figure

7.6-4 – never mind the dozens of frequencies in the 6 rectifiers of a three-phase bridge, in the example of Figure 7.6-3.

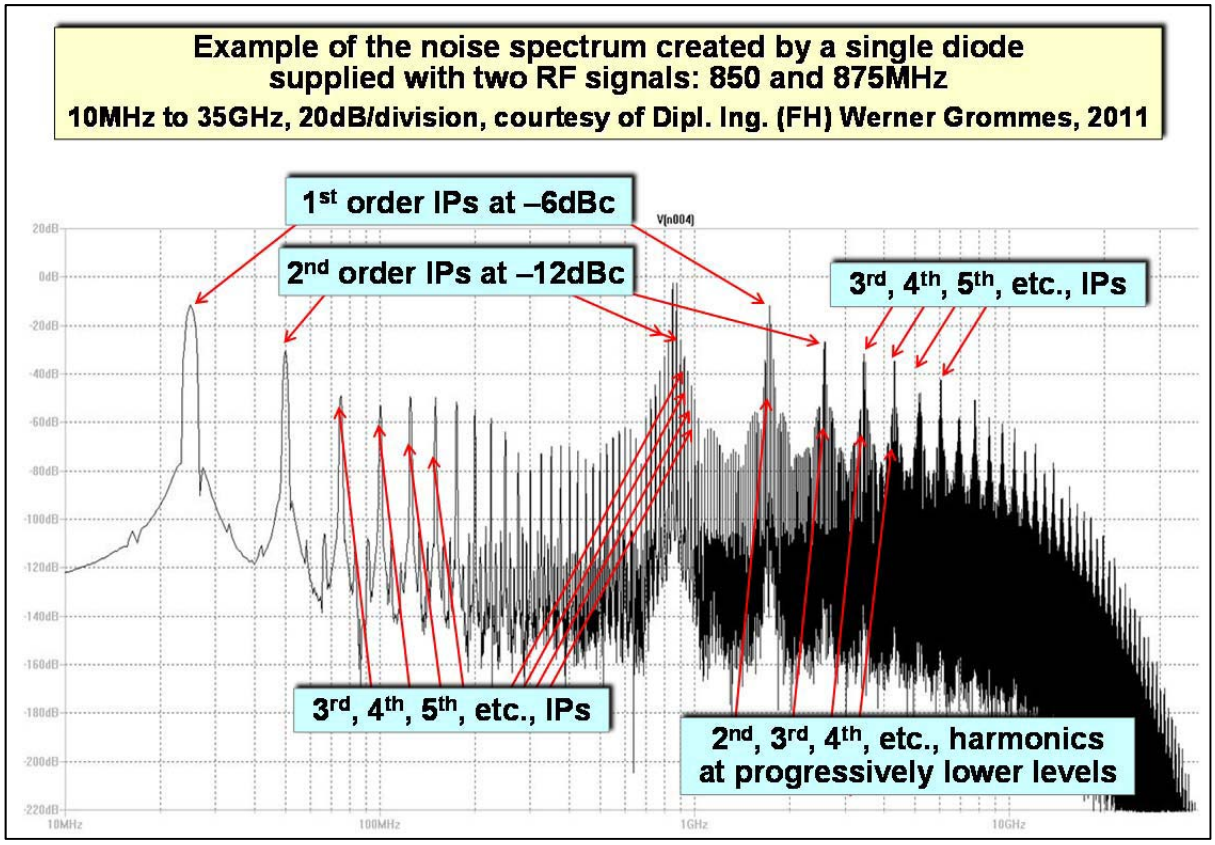


Figure 7.6-4 Intermodulation between 850MHz and 875MHz in a single diode

Frequencies as high as 850MHz are not (yet!) seen in switch-mode power converters, but the same results would have been achieved if the two frequencies in Figure 7.6-4 were 85Hz and 87.5Hz, or 85kHz and 87.5kHz – the only difference would be the frequency scaling of the horizontal axis.

7.6.2 Filtering techniques for DC

The cable shielding techniques described in [92] can be applied to DC inputs and outputs just as well as to AC outputs.

Applying them to AC mains power supply inputs is more awkward, because of the difficulties of 360°-bonding cable shields to the metal cases of AC mains distribution transformers, which are not a properly shielded boxes anyway because of the other unshielded and unfiltered cables that enter or exit them (cost-effective design of shielded enclosures is covered in Chapter 6 of [5]).

But the topic here is *filtering* DC power, and all of the filtering techniques discussed in the previous two articles [72] and [84] can be applied just as well to DC, as to AC power inputs and outputs.

The amount of charge stored in the filter or storage capacitor is one of the key issues in reducing power converter emissions at the switching frequency (and its harmonics), and results in a noise voltage often called “ripple” – an AC waveform riding on the DC voltage level.

Ripple noise voltage is obviously an important issue for DC inputs and outputs, and it is also an important issue for internal DC-Links.

A helpful and simple equation for the change in voltage on any capacitor is $C\Delta V = I_{AV}\Delta t$, where C is the capacitor’s value in Farads, ΔV is the change in voltage on the capacitor caused by the average current I_{AV} Amps flowing during the time period Δt seconds.

So, for example, a perfect 1000µF capacitor that is being charged or discharged by a current with an average value of 25 Amps during a time period of 1µs, will experience a change of 0.025V from whatever its voltage was originally. On this basis, it seems possible to arbitrarily decrease the noise voltage by simply increasing the capacitor value to whatever value is necessary.

But a capacitor is not simply a capacitor! Real components are never ‘pure’ – as simple circuit simulators assume – and Figure 7.6-5 shows a 1st-order approximation of what we actually get when we purchase a

capacitor, rather than an idealised capacitor that cannot possibly exist in this universe. This figure is based on an electrolytic capacitor, but exactly the same analysis applies to all non-polarised capacitors too.

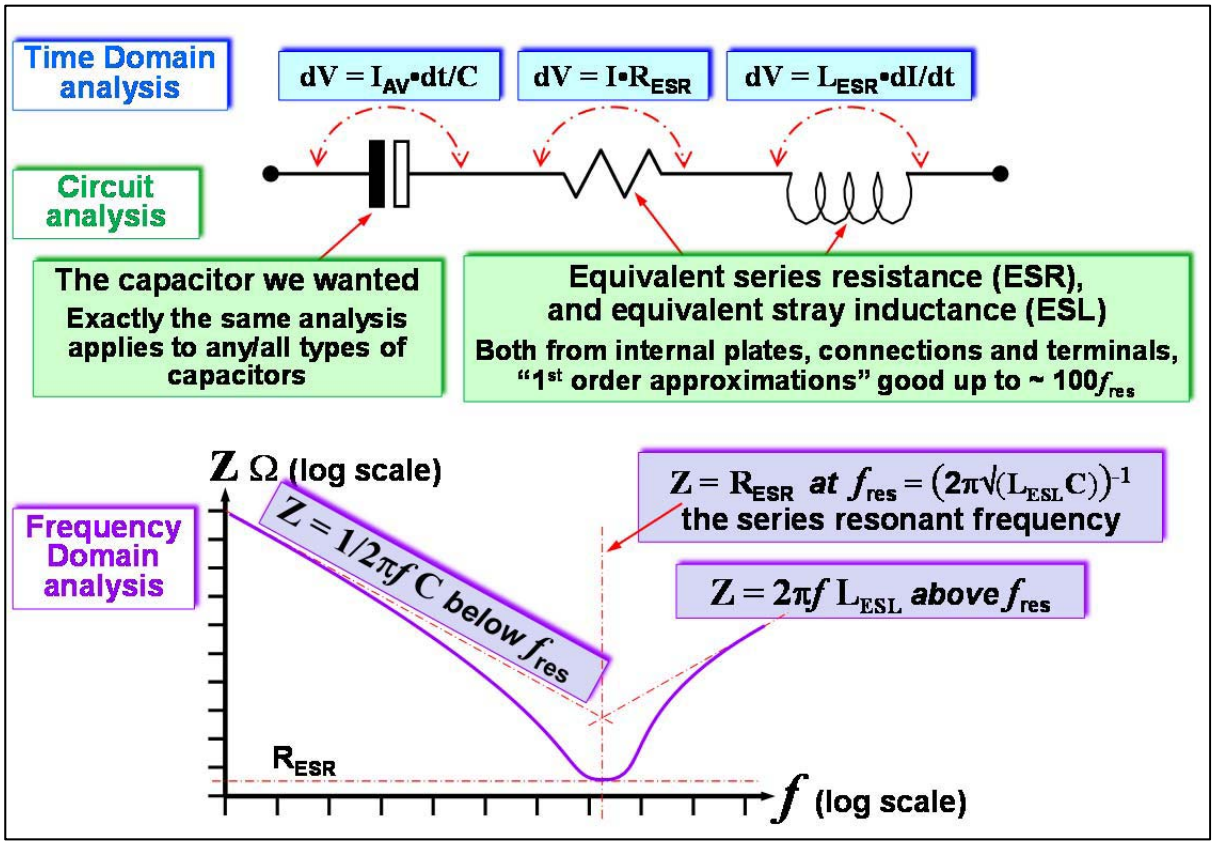


Figure 7.6-5 A 1st-order equivalent circuit, showing that real capacitors are complex

The circuit analysis in Figure 7.6-5 shows that the real capacitors that we assemble our products from all suffer from "pollution" caused by their Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL). The simplified time-domain and frequency-domain analyses on this figure show what we should expect when we pass switching currents through capacitors.

(There is also a leakage resistance bypassing the capacitor, but it is only important for precision sample/hold analogue circuits, and where a circuit must run from the energy stored in tiny batteries, or capacitors, for long periods of time, so I ignore it in this article.)

The ESR and ESL limit the effectiveness of the DC-Link (= DC storage) capacitor as a filter, but even adding low-value non-polarised capacitors in parallel doesn't always help as much as we might hope, because they also suffer from ESR and ESL.

Also, paralleling capacitors adds a totally new problem for ripple voltage reduction: the capacitors' ESLs cause *parallel* resonances to arise, which have very *high* impedances (see 7.6.3 below) – not what we want for low emissions!

Like many designers, I have happily paralleled all sorts of types and values of capacitors without suffering any surprise ill effects. What this means is that the parallel resonances thus caused did not happen to coincide with the switcher's fundamental frequency or any of its harmonics.

Murphy's Law [93] tells us that paralleling capacitors with no regard to the high-impedance resonances thus caused will be just fine, until some years later when we are asked to make a small increase in the switching rate (maybe to save cost by reducing the size of the magnetic components).

This simple task that the designer's boss expects to take a few hours can cause either the fundamental frequency or a harmonic to "just happen" to coincide with a parallel resonance in the DC-Link or filter capacitors. It is not unusual in such situations for the conducted mains emissions at that new frequency to suddenly shoot up from nowhere, to 20dB or more above the limit line.

Of course, the reason for this isn't obvious to the poor designer, and his boss can't understand how he or she could have made such a simple job take so long. Murphy's Law is the bane of all designers, but no-one has yet found a way of getting around it. (Actually I once did, and might write about it one day.)

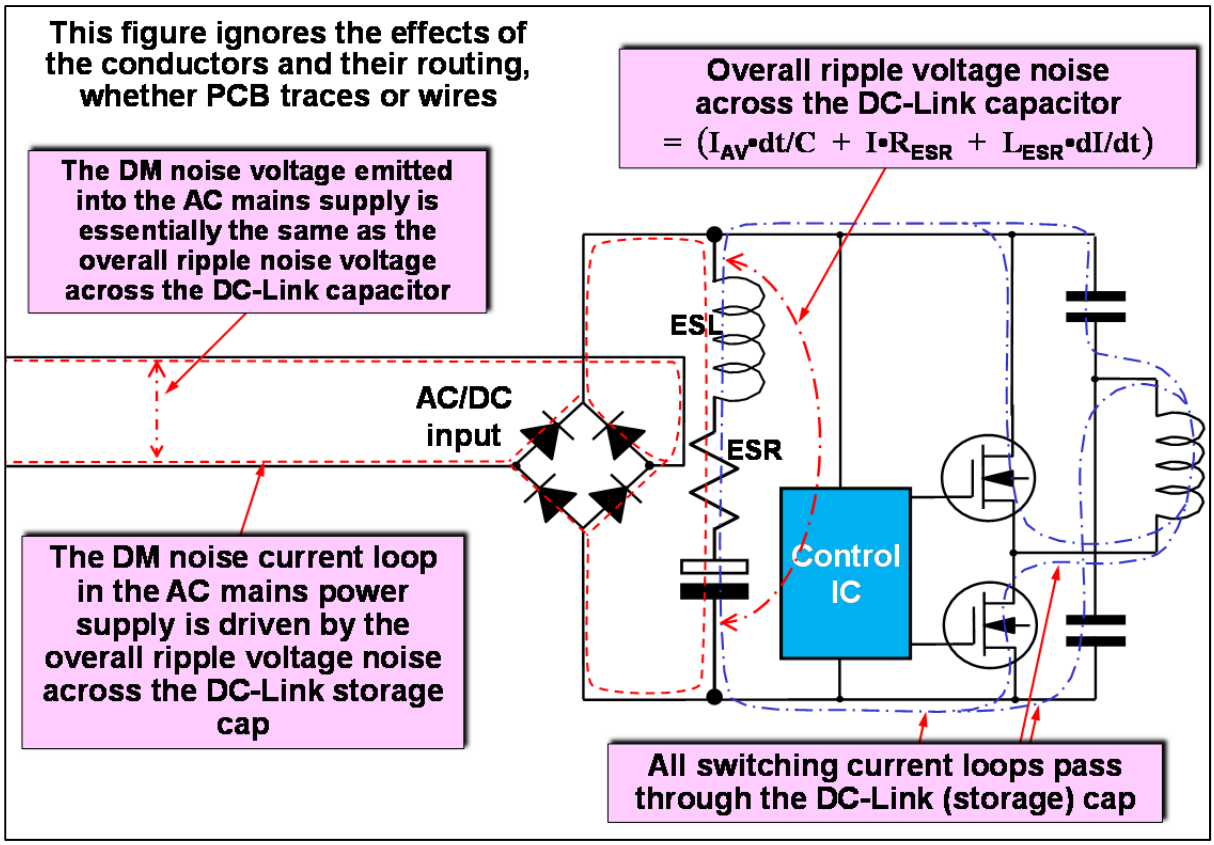


Figure 7.6-6 Showing how the ripple voltage directly influences conducted emissions

Figure 7.6-6 is an example that attempts to show how the ESR and ESL in a DC-Link capacitor increase the ripple voltage noise, and how this drives a differential mode (DM) noise voltage and current through the bridge rectifier and into the AC or DC power supply. This figure is based on a half-bridge switcher, but applies to any/all kinds of switchers that have a DC-Link.

This figure doesn't show the mains filter that will be needed to suppress this DM noise, and the common-mode (CM) noise caused by the noise current flowing in the (unbalanced) power supply distribution network. In power input and output filters (see 7.3 in [72] and its continuation in [84]) exactly the same problems are created by the ESR and ESL of the filter capacitors, whether the power supply is DC or AC.

It is generally more cost-effective to suppress conducted power supply emissions at their source (i.e. the ripple noise voltage on the DC-Link capacitor) than it is to suppress the noise in the AC or DC power supply conductors, and this was the basis for my one-capacitor modification to the military submarine winch motor drive, that I described in 7.3.8 in [84].

From Figure 7.6-5 we can see that the overall impedance of a capacitor, Z_{CAP}, is:

$$Z_{CAP} = \{(j/2\pi f \cdot C) + (-j2\pi f \cdot L_{ESL}) + (R_{ESR})\}$$

(Remember, this uses a 1st-order approximation that is probably only good to around 100 times f_{RES}).

Purists will note (hopefully with approval) that I have included the phase-angle operator, j, in the above equation. When I was a student this used to terrify me because it was the square root of minus one, and therefore an imaginary number, and my AC circuit theory tutors used to refer to "imaginary" voltages, currents, impedances, and even "imaginary" electrical power (i.e. 'wattless power')!

But all it means in practice (i.e. the real world) is that any quantity multiplied by j has a phase-angle that is 90° ahead (i.e. 'leading'), whereas one multiplied by –j has a phase-angle that is 90° behind (i.e. 'lagging'), and you can see these phase angles clearly on any oscilloscope, there is nothing imaginary about them at all!

The reason for the "square root of minus one" aspect of j becomes apparent when you set the capacitive current in a circuit exactly equal to the inductive current, and so achieve a series or parallel resonance – in which situation the circuit has only the characteristics of resistance. Try it, in the above equation for a 1st-order approximation of a capacitor, and prove it for yourself.

(Without considering the +j and –j phase angles associated with the capacitive and inductive impedances, resonance cannot occur, and we could never have made any tuned circuits and so could never have been able to tune to different radio frequency "channels").

When selecting DC-Link capacitors, a large value of capacitance is generally aimed for, to provide a low impedance at the fundamental switching frequency. But, above some number of µF, diminishing returns set in because the R_{ESR} value becomes larger than the value of $1/2\pi f \cdot C$. So we need a very low ESR, to reduce the ripple and emit less noise.

The above assumes that the fundamental frequency of the switcher is so low that the effect of the ESL is negligible, which is not always the case. In some applications the ESL is high enough that $2\pi f \cdot L_{ESL}$ can equal or exceed the value of $1/2\pi f \cdot C$ and/or R_{ESR}. So we sometimes also need a low ESL to suppress the fundamental frequency.

The same considerations apply to suppressing the harmonics of the switching frequency, and of course as the frequency increases the impedance due to $1/2\pi f \cdot C$ reduces whilst the impedance due to $2\pi f \cdot L_{ESL}$ increases, eventually – above some frequency – making the ESL the dominant, most important, issue for suppressing ripple voltage and noise emissions.

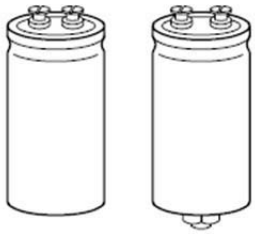
The current flowing in the ESR of a capacitor results in "I^2R" heating that can be so large that it shortens the life of the capacitor, especially wet electrolytic types through drying out of their electrolyte. This is why – if an operational life of more than a few months is required – it is so very important to choose electrolytic capacitors with ambient temperature ratings, plus ESRs and ripple current ratings that the design will not exceed.

This heating issue is especially important for high-power converters, and later on I will briefly discuss some special capacitor types that have been developed to have very low ESRs and very low self-heating in such situations.

It is always tempting to try to choose a DC-Link capacitor that has its series resonance at the fundamental frequency, although where this lies below the lowest frequency tested by the so-called "CE marking" standards many designers will instead try to series-resonate their DC-Link capacitance at the first harmonic that equals or exceeds the lowest tested frequency. (The wisdom, or not, of ignoring emissions that lie below the tested frequency range is discussed later).

Let's take a practical example of a capacitor that – at the time of writing – is supplied as being suitable for use as the DC-Link in a switch-mode power converter, the EPCOS (TDK) B43455A5158M000: 1,500µF, 450Vdc, rated 10,000 hours life at 85°C, aluminium electrolytic with screw terminals, see Figure 7.6-7. Please note that I am not recommending this type of capacitor, it's just the first one I came to when flicking through a distributor's catalogue to find an example to use in this article.

From the EPCOS data sheet for the B43455 and B43457 General-purpose grade capacitors sold as being suitable for use in: uninterruptible power supplies; frequency converters, and professional power supplies



KAL0567-B

B43455 B43457

Technical data and ordering codes

U_R VDC	C_R 100 Hz 20 °C µF	Case dimensions $d \times l$ mm	ESR_{max} 100 Hz 20 °C mΩ	Z_{max} 10 kHz 20 °C mΩ	$I_{\sim max}$ 100 Hz 40 °C A	$I_{\sim max}$ 100 Hz 85 °C A	$I_{\sim R}$ 100 Hz 85 °C A	$I_{\sim R}$(B) 100 Hz 85 °C A	Ordering code[1]
450	470	51,6 × 80,7	390	420	7,0	3,1	2,6	4,1	B4345*A5477M000
	1 000	51,6 × 80,7	180	200	12	5,1	4,2	8,6	B4345*B5108M000
	1 500	64,3 × 105,7	120	130	16	6,9	5,8	9,4	B4345*A5158M000[2]
	2 200	64,3 × 105,7	81	70	18	7,9	6,6	12	B4345*B5228M000[2]
	3 300	76,9 × 143,2	54	48	25	11	9,1	14	B4345*A5338M000[2]
	4 700	76,9 × 220,7	42	39	31	14	11	15	B4345*A5478M000[2]
	4 700	91,0 × 144,5	42	39	31	14	11	19	B4345*J5478M000[2]
	6 000	76,9 × 220,7	33	31	38	17	14	19	B4345*A5608M000[2]
	8 200	91,0 × 221,0	24	24	48	21	18	25	B4345*A5828M000[2]

Figure 7.6-7 Some data on the EPCOS B43455 capacitor range

And let's also assume that it is used as the DC-Link that follows the bridge rectifier in a 230Vac rms input 300W output switching power converter similar to the half-bridge type sketched in Figure 7.6-6, with a switching frequency of 51kHz.

The storage capacitor is nominally charged up to 325Vdc and experiences a sawtooth current waveform into the switching devices with an RMS current of, say, 1A and a peak current of 2A.

Now, I know that your current project has a different switching waveform so has a frequency spectrum that is very different from a sawtooth wave, and has different voltage and power requirements, different switcher type, different everything, but this is just a simplified example to help us discuss the issues associated with the value, ESR and ESL of the DC-Link capacitor.

A sawtooth wave can be "decomposed" into frequencies using Fourier analysis [94], as follows: Fundamental -1/2(2nd harmonic) + 1/3(3rd harmonic) – 1/4(4th) + 1/5(5th) – 1/6(6th) + 1/7(7th)….etc., up to a very high frequency limited by the rise and fall-time of the switching devices (almost certainly exceeding 51MHz in a converter of this rating).

Because the harmonics alternately add and subtract, to achieve our overall current of 1A rms and 2A peak, the current at the fundamental frequency has to be a little larger, and I have estimated it at 1.5A rms and 3A peak.

Knowing the currents at the fundamental and harmonic frequencies, we *could* calculate the various contributions to the ripple noise voltage across the 1500µF capacitor from the three components of the 1st-order approximation equivalent circuit shown in Figure 7.6-5, remembering to take into account their various phase angles. Instead, EPCOS have provided us with a handy graph of overall capacitor impedance (Z) versus frequency, which is copied in Figure 7.6-8. This graph implies an ESR of about 30mΩ, an ESL of about 16nH, and although the series-resonant frequency would be expected to occur around 32kHz, the graph shows that it actually occupies quite a wide range, approximately from 3kHz to 200kHz.

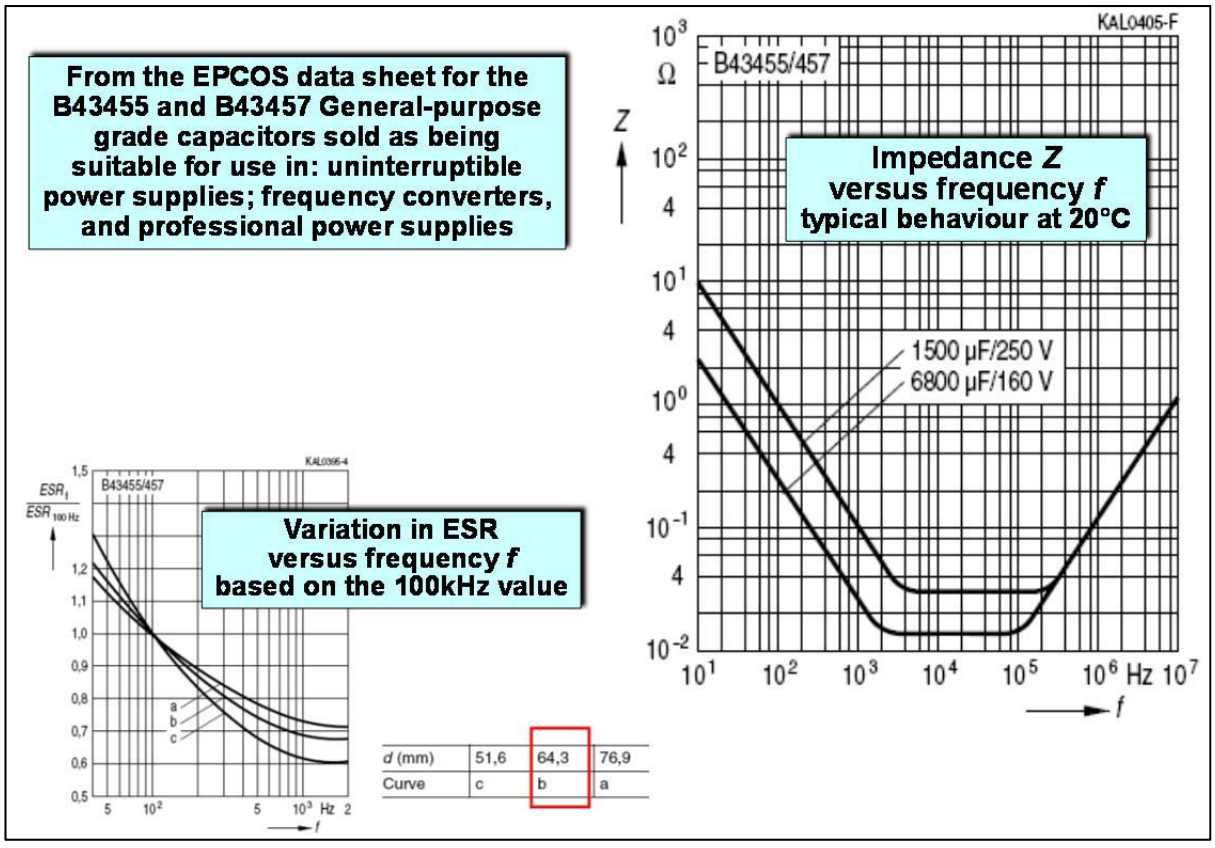


Figure 7.6-8 Variation of overall impedance with frequency, for the B43455 capacitor range

Using this handy graph and the harmonic series for our sawtooth current waveform, for our example 300W switcher we can say that its DC-Link capacitor will experience (approximately) the peak currents and develop the peak noise voltages as listed in Table 7.6-1.

Measuring the conducted emissions of a product adds a CISPR-specified LISN in series with its power supply, which sources the power from an impedance of 50Ω in the range 150kHz to 30MHz.

However, the source impedance of the DM ripple noise voltage is the impedance of the DC-Link capacitor at the frequency concerned, which we can see from Figure 7.6-8 is always less than 3Ω between 100Hz and

30MHz. So we can assume that the noise voltage on the DC-Link capacitor will not be significantly attenuated by the LISN's 50Ω, and will be what is measured by a receiver or spectrum analyser.

Because the fundamental frequency and its harmonics are fixed (i.e. they are not using spread-spectrum or chaotic techniques to reduce emissions by "smearing" them widely over the frequency spectrum, see 2.8 in [42]), when tested for conducted emissions they will measure almost exactly the same when using the measuring receiver's Peak detector as they will using its Quasi-Peak detector.

This means we can compare our peak noise voltage calculations with the Quasi-Peak limits in the relevant emissions test standards, such as CISPR 22 (EN 55022) and CISPR 11 (EN 55011) to see how much filtering would be required for our 300W converter to pass their conducted emissions test.

Note that in the final column of Table 7.6-1, I am aiming for 6dB below the limit line. This is a good practice to help ensure that component tolerances and assembly variations don't result in non-compliant products being sold during serial manufacture.

Relationship	Frequency kHz	Peak Current Amps	Capacitor impedance Z Ω	Peak voltage noise across the capacitor μV (dBμV)	Filtering required *to be 6dB below* the "Class B" Quasi-Peak conducted emissions limit line
The switching frequency	51	3.0	0.03	90,000 (99)	n/a (no limits < 150 kHz)
2nd harmonic	102	1.5	0.03	45,000 (93)	n/a (no limits < 150 kHz)
3rd harmonic	153	1.0	0.03	30,000 (90)	30dB
4th harmonic	204	0.75	0.03	22,500 (87)	30dB
5th harmonic	255	0.60	0.04	24,000 (88)	33dB
10th harmonic	510	0.30	0.06	18,000 (85)	35dB
98th harmonic	4.99 MHz	0.03	0.6	18,000 (85)	35dB
588th harmonic	29.99 MHz	0.0051	3.0 (extrapolated)	15,300 (84)	30dB

Table 7.6-1 Analysis of noise spectrum of the ripple voltage

Table 7.6-1 is not precise, and I am particularly worried by the fact that the datasheet lists the 1500μF capacitor's Z as being a maximum of 130mΩ at 10kHz (see Figure 7.6-7) whereas the graph provided by the same datasheet (see Figure 7.6-8) shows it as typically being about 30mΩ at 10kHz.

The difference between 130mΩ and 30mΩ is about 12dB, so it seems that to be sure of complying with the EMC Directive in serial manufacture despite tolerances in capacitor ESR and ESL and still have a few dB "margin" for other parameter tolerances, we should increase the filtering figures in the right-hand column by 12dB.

We haven't even asked how the capacitor impedance varies with temperature, and all the figures we have used so far are based on its datasheet specifications at 20°C. Most likely, once we have investigated temperature coefficients, we will find that when our capacitors are running at between 40°C and 60°C, as they will most of the time in this example, we will need to add another few dBs of attenuation to our filtering.

We can say then, in round numbers, that we are aiming for 50dB of differential-mode attenuation from our filter, in order to meet Class B conducted emissions limits. For Class A, we can (rather crudely) assume that about 37dB of filter attenuation would be needed.

If, instead of choosing the 1500μF capacitor from the B43455 range we chose their 6800μF one, the impedance below 100kHz would reduce from about 0.03Ω to about 0.012Ω, i.e. by about 8dB, but this size increase would only help the 3rd and 4th harmonics of our 51kHz switcher comply with the conducted emissions limits.

If we could reduce the capacitor's impedance over the frequency range by, say, 20dB, we could reduce our filtering requirements by the same amount. Spending more on the DC-Link capacitor might well result in an overall cost saving, by reducing the cost of the power input filter (see [12]).

One good way of reducing capacitor impedance is to use many smaller capacitors in parallel. This is because quite a lot of the impedance (ESR, ESL) in a capacitor comes from the way the metallised foils that create the actual capacitance are connected to its terminals, plus the terminals themselves. Paralleling many capacitors also parallels the ESRs and ESLs of these interconnections, and so has a better effect overall.

For example, paralleling four 1500µF B43455 capacitors to give us 6,000µF should result in an impedance versus frequency curve that is one-quarter of the 1500µF curve in Figure 7.6-8 over the entire frequency range to 30MHz, whereas the single 6800µF capacitor in that same range only shows an approximately quarter impedance up to 200kHz.

So, using four 1500µF B43455 capacitors in parallel (using good PCB layout / planar bus structures / cabling discussed in the next issue of this series) should reduce our power-input filtering requirements by 12dB over the frequency range 150kHz to 30MHz, i.e. from 50dB to 38dB.

Ten such capacitors in parallel would win us 20dB, reducing the filtering specification for Class B conducted emissions to 30dB, and for Class A to 17dB.

For other viewpoints on DC-Link capacitor selection, see [95] and [96]. [95] focuses on low-power board-mounted switchers, but its principles can be applied at any power level. It sings the praises of ceramic and tantalum capacitors, and I have used dozens of large ceramic capacitors in parallel to provide low DC-Link impedances at 28Vdc for power converters used in aerospace applications.

[96] compares aluminium electrolytic capacitors with ECI's proprietary polypropylene film capacitors in high-power inverters, for example as used in wind turbines. These non-polarised types are available with values of up to 300µF with voltages up to 2.2kV, and Figure 7.6-9 shows some examples of them.

From the ECI data sheet for their UL3 series "Unlytic" series of polypropylene film capacitors intended for high-power DC filter applications up to 105°C

UL31, 32, 34 AND UL35

ELECTRICAL SPECIFICATIONS

				ESL FOR UL31 AND UL32		ESL FOR UL34 AND UL35				
										IN CIRCUIT
PART NUMBER	VOLTAGE	VALUE	CASE "H"	"L"	Fres	"L"	Fres	I pk	dv/dt	E.S.R.
	VDC	uF	mm	nH	kHz	nH	kHz			mOHMS
UL3_Q157K	500	150	40	25	82.2	12	118.6	5769	38	0.47
UL3_Q207K	500	200	51	32	62.9	15	91.9	5809	29	0.57
UL3_Q277K	500	275	64	50	42.9	25	60.7	5672	21	0.77
UL3_Q307K	500	300	79	55	39.2	27	55.9	5022	17	1.70

Figure 7.6-9 Some information on the ECI 'Unilytic' range of film capacitors

One of the most important issues for high-power converters, such as those used in electricity generation (e.g. wind turbines) and for motor control in electric or hybrid vehicles, is heating, which (as mentioned before) is only caused in capacitors by the I^2R effects of the ripple current flowing in the ESR. This concern is very plain in [96], and it is also a major consideration in [97] and [98], which discusses another proprietary film capacitor construction intended for high-power converters – SBE's Power Ring Film Capacitor™, some examples of which are shown in Figure 7.6-10.

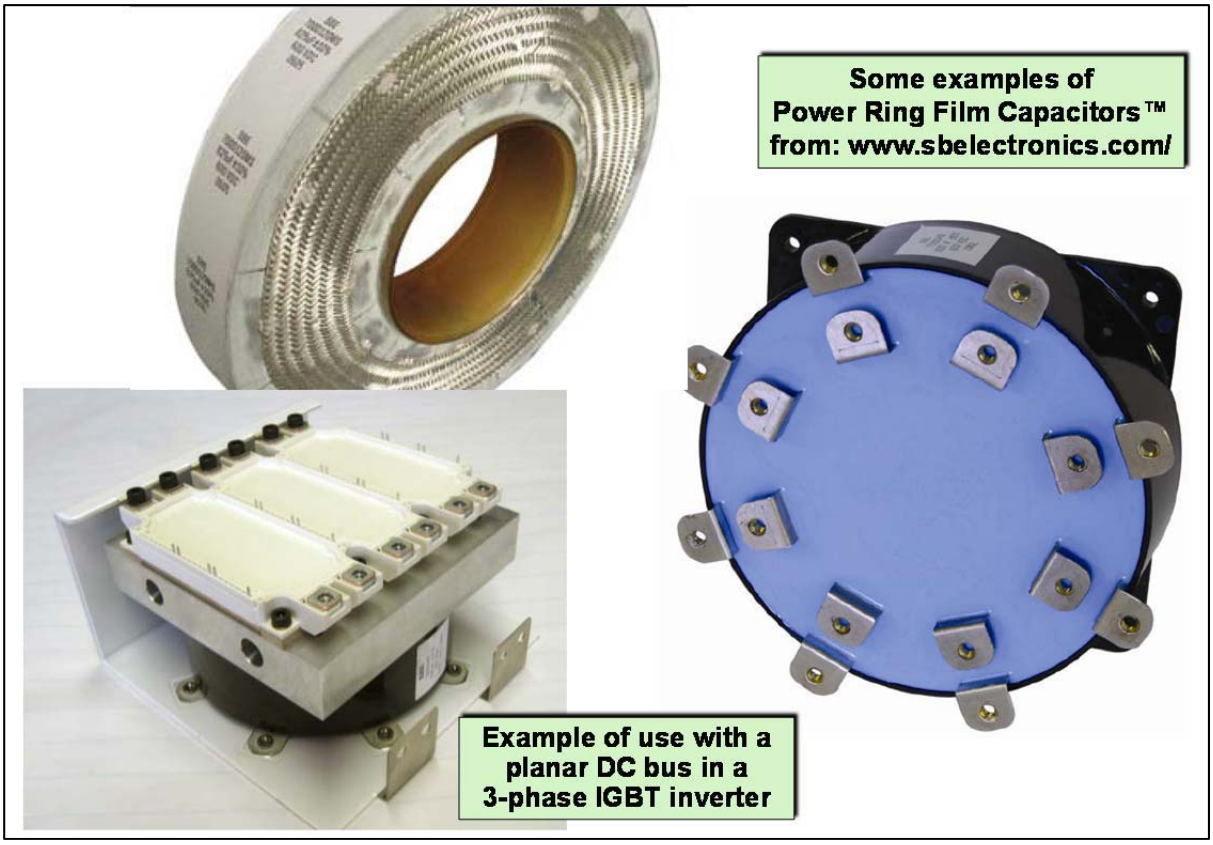


Figure 7.6-10 Some pictures of SBE's Power Ring film capacitors

[97] says that it shows that a 1000μF 600V Power Ring Film Capacitor with a "properly designed terminal structure" (such as the one on the right of Figure 7.6-10) can have an ESL of approximately 3nH.

[97] shows an example construction for a three-phase IGBT inverter, that I have copied bottom-left in Figure 7.6-10, and says that with careful design of a planar DC bus structure, this total package can achieve an ESL of approximately 20nH, with most of this forced on the structure by the non-optimal way the IGBT packages' terminals are arranged. The overall impedance of the DC bus is important for overshoots in the switching waveform delivered to the load, but with good design of the PCB/planar bus/cabling (which will be covered in the next issue in this series) its significance for conducted emissions on the power input can be reduced to nearly zero.

[97] gives no figures for ESR, and neither does [98], but [98] does mention that the heat generated within SBE's 700D348 1,000μF capacitor when it is carrying 200A rms is less than 6W (!), and from this we can estimate the ESR as 0.15mΩ. This is a very low ESR indeed.

So, using this model of 1,000μF capacitor in our example 300W converter above, plus good design techniques for the converter's PCB/planar bus/cabling (see the next issue) to achieve a DC-Link capacitor with an ESR of 0.15mΩ and an ESL of 3nH, we could reduce the emissions listed in Table 7.6-1 by about 46dB around 150kHz, reducing to about 15 dB at 30MHz.

This could reduce the filtering specification over the range 150kHz to 30MHz from 50dB overall for Class B, to a filter that attenuates progressively from 0dB at 150kHz to 35dB at 30MHz.

Class A would only need a power input filter that attenuated from 0dB at around 2MHz up to about 22dB at 30MHz.

Of course, in the above I have ignored the cost/benefit analyses that every engineer needs to do. It is almost certain that, for our above example 300W converter, the use of the proprietary power film capacitors such as those in figures 7.6-9 and 7.6-10 would be a costly overkill, and it might even be the case that using four 1500μF B43455 capacitors in parallel would be more costly than providing the 12dB of filtering they replaced – especially since some sort of power input filtering is certain to be required anyway.

However, it is important to remember that, in real-life, filters resonate (see 7.3.7 through 7.3.9 in [84]) and providing a reliable 50dB of attenuation from 150kHz to 30MHz in real life is often not as easy as distributors' catalogues of filters make it seem (as proven by my story about suppressing the emissions from a submarine winch motor drive, that I described in 7.3.8 in [84]).

Also, a 1500µF DC-Link capacitor might not provide sufficient hold-up time to cope with AC mains supply dips, dropouts and short interruptions.

Assuming that the permissible DC-Link voltage droop during an interruption is 50V (e.g. from 325Vdc to 275Vdc) a 1500µF capacitor would only supply 1A rms for 75 ms, whereas the generic immunity test standard IEC/EN 61000-6-1 (for domestic, commercial and light-industrial environments) applies 60% dips lasting for 5 mains cycles (i.e. 100ms). The heavy industrial version (IEC/EN 61000-6-2) adds tests with 60% dips for 50 cycles (1 second).

So it might turn out that spending more money on the DC-Link capacitor is cost-effective after all!

Some experimentation (with measurement of conducted emissions) or simulation is clearly generally required, to be sure of making the correct decisions early in the project (when design changes are effectively free), instead of struggling to pass EMC tests at the end of a project, when design changes are very costly indeed and many of the most desirable design changes are not even practicable (see the introduction to [91]).

7.6.3 Circuit simulation techniques

The only way to get switched simulation results that bear some resemblance to real-life circuit operation and filter attenuation and resonances, is to include 1st-order (at least!) effects like ESR and ESL in them.

This can be done by making these non-idealities part of the component specifications, so that each time we add a capacitor chosen from the component library we actually import a complex circuit like that shown in Figure 7.6-5. Alternatively we can actually draw the 1st-order approximated circuit for each component and enter the appropriate values for ESR and ESL.

Data on the first-order approximated characteristics should be available from the datasheets of reputable manufacturers, and we should never attempt to design any switching circuit without it.

Although I am discussing capacitors here, the same issues of including 1st-order approximated equivalent circuits for each component, applies to all of the passive and active components in the circuit, especially the switching devices, where they will help predict overshoots and ringing that may need snubbing or modifications to the circuit design or component choices.

In the mid-late 1980s I was managing a new product design project in a large (for the UK) company, and we purchased a simulator. Its 500MB hard-drive was the size of a small domestic oven, which shows how far technology has progressed in 30 years. The product used a 200W 25kHz sine-wave inverter, which proved quite difficult to get working properly. This inverter was the first thing we simulated with our new toy, but when we saw that it was predicting five switching edges at each switching transition, we couldn't see how this could possibly occur and assumed the simulator was giving silly results.

So we ignored the simulator and designed the inverter the good old-fashioned way, with a limited understanding (we didn't realise how limited, of course, until later on) and a lot of trial and error using prototype constructions. It took us 6 months of frustration to discover that the circuit really was switching five times (very quickly indeed!) for every once that we wanted it to.

Once we realised that this extra switching was a real problem, we very quickly learned what was causing it and the design then started to make good progress. But the true cost of the 6 months delay in that part of the project was about the same as the purchase price of what was generally considered to be a very expensive state-of-the-art simulator!

To prove the value of including at least the 1st-order approximated equivalent circuit components in a circuit simulation, try simulating 100µF in parallel with 1µF and measuring how their combined impedance varies with frequency – firstly as ideal (perfect) capacitances – and then with their ESRs and ESLs added in, which reveals the high-impedance parallel resonance. Dramatic, isn't it!

Figure 7.6-6 and this article ignore the effects of the conductors and their routing, whether they are PCB traces, planar bus structures or wires. These non-idealistic effects of what are basically conductors are never covered by circuit simulators, although some simulators can be linked to 3-D field solvers to extract the relevant parameters from the field solver and import them into the circuit simulator.

Updating a circuit simulator's schematic with the "construction parasitics" extracted from a 3D field solver makes it possible, after some iteration of the design, for a simulation to *virtually* guarantee all aspects of switcher operational performance *and* its conducted emissions *before the first prototype is made*.

This is essentially the way that manufacturers of personal computer motherboards, which have a sales life of less than 90 days, ensure their products are "right first time" for functionality and EMC.

The computer software necessary to perform such wonderful feats is not cheap (most people laugh loudly when told the price!) – but in fact it is easy to make a good business case that shows such software should pay back its purchase price on the next project, never mind the 3 years that the usual business plan considers acceptable.

7.6.4 Reducing emissions at frequencies below 150kHz

Many designers are encouraged by their managers to only do the minimum for EMC, because they think it is only a regulatory compliance issue – they don't realise that good EMC is an essential part of how their products are perceived by their customers, and can have a strong negative effect on the cost of sales, the financial success of a product, and (eventually) on the manufacturer's market share.

I have seen 50kW variable-speed motor drive conducted emissions at around 20kHz ruin the control of most of the other equipment in a factory. The 5th harmonic of the 4kHz-switching motor drive was amplified by a natural 'parallel' resonance of the factory's mains distribution network around 20kHz, creating about 20 volts peak-to-peak all over the site.

Fitting a better mains filter (interestingly, the one recommended by the drive manufacturer (Siemens) rather than the custom-designed one that had the lowest cost whilst still complying with the emissions standards above 150kHz) solved the problem, but not before the very costly new machining centre containing the drive had been unable to be used for nearly 6 months, at a great loss to production and great financial loss to the user.

And I have seen 1kHz - 20kHz (fundamental plus harmonics) emissions from 700kW AC motor drive cause large offshore drilling platform cranes to go out of control, creating serious safety hazards and costing the manufacturer US$54 million overall. They thought they had been clever in saving costs on EMC, but – even with a discounted cash flow analysis – the $54 million this single project cost them due to EMI far exceeded what they had "saved on EMC" over the previous decades, never mind the loss of market reputation.

So when designing power converters (at least those >1kW), it is best to suppress *all* emissions, however low their frequency, because:

a) we don't want to upset customers...

b) we don't want to cause safety hazards...

c) complying with the European EMC Directive requires not causing unacceptable interference *at any frequency*...

This last point is worth expanding upon. Article 10 ("Safeguards") in the EMC Directive 2004/108/EC makes it perfectly plain that a product can comply with all the emissions tests and so achieve a "presumption of conformity" and affix the CE mark, but still face legal action if it actually causes interference in real-life.

However, the cost of any enforcement action usually pales in comparison to the commercial costs of having supplied products that cause EMI problems for their users, especially if there are safety implications, like the offshore platform crane example above.

References (for this article only)

[4] "The Physical Basis of EMC", Keith Armstrong, Armstrong/Nutwood UK October 2010, ISBN: 978-0-9555118-3-7, from www.emcacademy.org/books.asp. The same material is presented as Chapter 2 in [5].

[5] "EMC Design Techniques for Electronic Engineers", Keith Armstrong, Armstrong/Nutwood UK Nov. 2010, ISBN: 978-0-9555118-4-4, from www.emcacademy.org/books.asp.

[11] "When the going gets tough – smarter design wins", Keith Armstrong, The EMC Journal, Issue 81, March 2009, pages 21-24, available from the archives at wwww.theemcjournal.com.

[12] "BOM cost and profitability", Keith Armstrong, The EMC Journal, Issue 82, May 2009, pages 32-34, available from the archives at www.theemcjournal.com

[13] "The EMC design of Switch-mode and PWM power converters", Keith Armstrong, The EMC Journal, Issue 93, March 2011, pages 26-34, available from www.theemcjournal.com

[14] Keith Armstrong's earlier articles are available from the archives at www.theemcjournal.com

[15] Textbooks by Keith Armstrong and others are available from www.emcacademy.org/books.asp

[42] "EMC Design of High-Frequency Power 'Switchers' and 'Choppers'", Keith Armstrong, The EMC Journal, Issue 94, May 2011, pp 39-50, available from the archives at www.theemcjournal.com

[64] "EMC Design of High-Frequency Power 'Switchers' and 'Choppers' – Design techniques for HF isolating transformers", Keith Armstrong, The EMC Journal, Issue 95, July 2011, available from the archives at www.theemcjournal.com

[65] “EMC Design of High-Frequency Power ‘Switchers’ and ‘Choppers’ – Design techniques for LF (mains) rectifiers”, Keith Armstrong, The EMC Journal, Issue 96, September 2011, available from the archives at www.theemcjournal.com

[66] “EMC Design of High-Frequency Power ‘Switchers’ and ‘Choppers’ – Design techniques for high frequency (HF) output rectifiers”, Keith Armstrong, The EMC Journal, Issue 97, November 2011, available from the archives at www.theemcjournal.com

[72] “EMC Design of High-Frequency Power ‘Switchers’ and ‘Choppers’ – Suppressing RF emissions from converter inputs and outputs”, Keith Armstrong, The EMC Journal, Issue 98, January 2012, pages 27-38, available from the archives at www.theemcjournal.com

[84] “EMC Design of High-Frequency Power ‘Switchers’ and ‘Choppers’ – Suppressing RF emissions from converter inputs and outputs”, Keith Armstrong, The EMC Journal, Issue 99, March 2012, pages 30-42, available from the archives at www.theemcjournal.com

[85] “Fundamentals of EMC Design: Our Products Are Trying To Help Us”, Keith Armstrong, Interference Technology Magazine, 04/03/2012, www.interferencetechnology.com/fundamentals-of-emc-design-our-products-are-trying-to-help-us-3

[92] “EMC Design of High-Frequency Power ‘Switchers’ and ‘Choppers’ – Shielding (screening) the power converter’s output cable”, Keith Armstrong, The EMC Journal, Issue 100, May 2012, pages 32-38, available from the archives at www.theemcjournal.com

[93] “The Truth of Murphy’s Law”, Keith Armstrong, The EMC Journal, November 2008, available from the archives at www.theemcjournal.com

[94] http://en.wikipedia.org/wiki/Sawtooth_wave

[95] “Input and Output Capacitor Selection” Texas Instruments Application Report, SLTA055, February 2006, by Jason Arrigo, www.ti.com/lit/an/slta055/slta055.pdf

[96] “Selecting Film Bus Link Capacitors For High Performance Inverter Applications”, Michael Salcone and Joe Bond, EMDC conference 2009, www.ecicaps.com/pdf/whitepapers/IEMDC_2009_11310_Final_Rev_4.pdf

[97] “Characterization of Equivalent Series Inductance for DC Link Capacitors and Bus Structures”, M.A. Brubaker, T. A. Hosking, and E.D. Sawyer, PCIM conference 2012, www.sbelectronics.com/wp-content/uploads/2009/11/PCIM_2012_Final-2.pdf

[98] “Low Inductance – Low Temp Rise DC Bus Capacitor Properties Enabling the Optimization of High Power Inverters”, Edward Sawyer, PCIM 2010, www.sbelectronics.com/wp-content/uploads/2010/05/PCIM_paper_May_2010.pdf