Another EMC resource
from EMC Standards

11 - Suppressing Electrostatic Discharge (ESD)

Helping you solve your EMC problems

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Module 11: Suppressing Electrostatic Discharge (ESD)

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Change Record: v2.1 to v2.5, March 2019

- **Footnote added to all slides: 'Cherry Clough Consultants confidential training material'**
- **All URLs / hyperlinks now activated**
- **Contents list was 11.0.2, now renumbered as 11.0.3**
- **New slide added as 11.0.2 (Good EM Engineering; De-Risking projects)**
- **Slides 11.1.2 and 11.1.4 improved**
- **New slides 11.1.5 – 7 added**
- **Slides 11.2.2 – 11.2.7 improved, and 11.2.5's position swapped with 11.2.7**
- **Slides 11.3.2 and 11.3.5 improved**
- **New slide 11.3.7 added (Preventing latch-up of Si-Ge microwave LNAs)**
- **Slide 11.4.2 *heavily* modified, and continued on to (new) 11.4.2a**
- **Slide 11.4.3 improved, and continued on to (new) 11.4.3a**
- **Slides 11.4.4, 11.4.7 - 10 improved. *Note: important improvements to 11.4.8 and 11.4.9***
- **Slide 11.4.11 moved to section 5 and renumbered as 11.5.6**
- **Slides 11.4.12 – 13 renumbered as 11.4.11 - 12**
- **New slides 11.4.13 – 11.4.16 added**
- **Slides 11.5.2 – 11.5.5 improved**
- **Slides 11.6.4 and 11.7.1 – 3 improved**
- **Slides 11.8.2 and 11.8.3 updated and improved, and new slide 11.8.4 added**
- **Slide 11.0.3 renumbered as 11.0.4, and moved to the very end**
- **Overall number of slides increased from 52 to 62**

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Good EM (electromagnetic) Engineering, and De-Risking new projects

- **Good EM engineering is cost-effective SI, PI, EMC design: well-proven to save time & money in all lifecycle stages, helping increase profits & reduce financial risks…**
  - **for all products, equipment, vehicles, systems, installations; etc., of any size, in all applications…**
    see www.emcstandards.co.uk/testimonials ***and Module 1***
    (especially 1.15, which is also in Webinar 1c; and 1.16 which is also in Webinar 1d)
- **Our courses (of which this is one) provide a complete set of good EM Engineering guidelines, that should *also* be used as an initial design checklist to De-Risk new projects:**
  any that can't or won't be followed identify a project risk!
  also see Module 1, section 1.16 (also in Webinar 1d)
  - **to adapt any λ-based design guidelines to different applications and/or different EMC test standards: see Module 1, section 1.18** ***(also in Webinar 1d)***

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Contents

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11. Suppressing ESD

11.1

ESD threats

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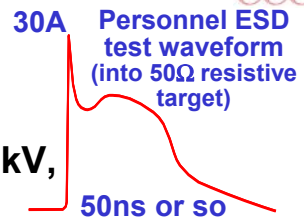
ESD threats



- IEC 61000-4-2 simulates personnel ESD by charging 150pF capacitor to 8kV, discharging it via a 330Ω resistor with rise-time 0.7-1ns, achieving 30A pk into a 50Ω target…
  - enough energy to damage semiconductors and even thin film resistors, also creating locally-intense E and H fields
- But real-life ESD not limited to personnel, can have: higher capacitance, lower series resistance, and/or…
  - up to 35kV (corona discharges prevent higher voltages)…
  - resonant waveforms with higher peaks than tested voltages…
  - faster risetimes than 0.7ns, especially for voltages < 4kV, down to 10ps (possibly less) at <100V with µm-sized gaps

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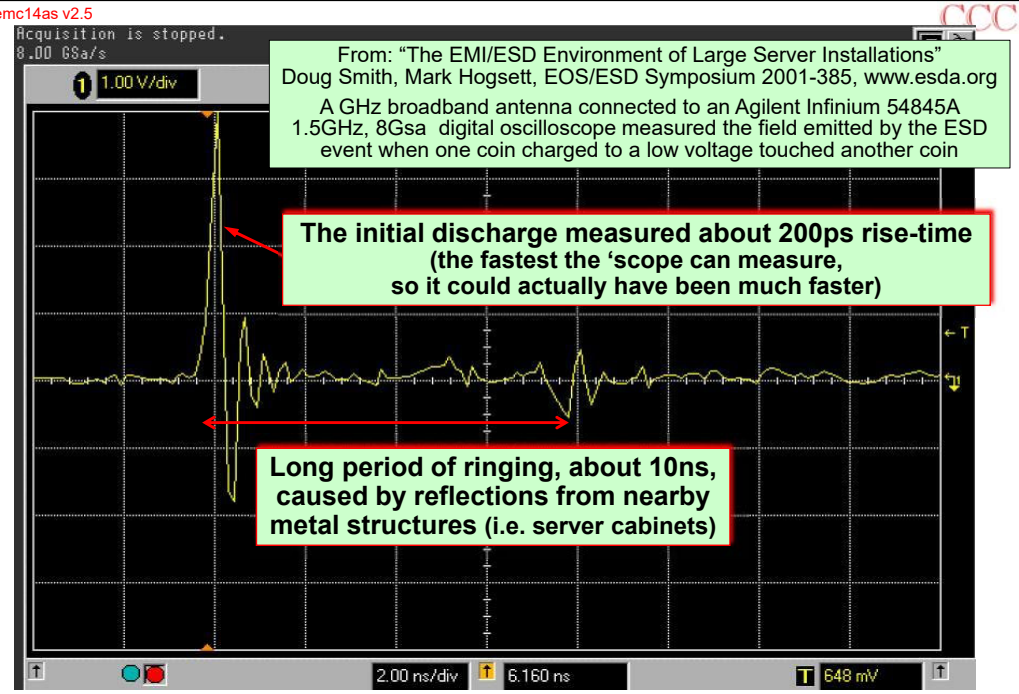

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Semiconductor die-shrinking is unavoidable (Google: Moore's Law) (1)

- **Their ever-smaller transistors can be upset by ever-shorter risetimes, and damaged by ever-lower voltages**
- **Their internal I/O protection diodes may be smaller, hence less effective…**
  - **or may even be omitted because they displace too many hundreds of millions of transistors!**
- **The result of die-shrinking is that ESD protection is continually getting ever-more difficult…**
  - **see for example Doug Smith's blog:** https://myemail.constantcontact.com/HFNews-for-January-20--2017--ESD.html?soid=1127008467999&aid=RmapKkRMm-A

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Semiconductor die-shrinking is unavoidable (Google: Moore's Law) (2)

- *In 2013, typical* digital ICs needed protecting against ESD with 100ps risetimes (i.e. ≥ 3GHz)…
  - in 2010, some fast CMOS chips responded to 50ps (i.e. ≥ 6GHz)…
  - – and peak voltages limited to < 10V (ideally: kept within the V+ and V- (0V, GND, etc.) power rails)
- In 2019 we should *typically* use ≤ 50ps (i.e. ≥ 6GHz)…
  - – *see Module 1 section 1.18 for how to determine the f_{MAX} for the ICs being (or to be) used*
    - future die-shrinking doesn't only affect new designs, it also affects products in serial manufacture – making them more susceptible to real-life ESD, every 2 years or so…
    - several manufacturers have suffered huge losses for this reason alone

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ESD testing with risetimes < 0.7ns

- In the 1980s, the IEC 61000-4-2 test *(equivalent)* used a 5ns risetime, reduced to 0.7-1ns in 1990s to cope with real-life effects of die-shrinking…
  - – unfortunately there are currently no plans to reduce it again to better suit real life in the 2020s
- Some ESD guns can test to different ESD standards by fitting different 'RC Modules' (Discharge Networks)…
  - – which might be available (or modifiable) to get shorter risetimes (e.g. try 200pF - 0Ω 'Machine Model' discharge networks)
    - e.g. the Thermo Keytek MinZap MZ-15 should achieve 150ps risetime with its discharge network shorted out