Another EMC resource
from EMC Standards

10a - Advanced PCB design techniques for cost-effective SI, PI and EMC

Helping you solve your EMC problems

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Module 10A (replaces Module 10)
Advanced PCB design/layout techniques for cost-effective SI, PI and EMC in 2019

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Change Record: v1.6 – v1.8, January 2019 (1)

- **Slides 10A.0.1a and 4 slightly modified** to update and communicate better
- **Slide 10A.2.4 updated**
- **Slides 10A.3.44 and 51 slightly modified** to communicate better
- **Slides 10A.4.2 and 3 slightly modified** to communicate better
- **Slides 10A.5.8, 16, 18, 23, 26, 33 and 34 slightly modified** to communicate better
- **Slides 10A.5.23a and 31 updated**
- **Slide 10A.6.7 slightly modified** to communicate better
- **Slides 10A.6.11 and 12 swapped: renumbered as 10A.6.12 and 11 respectively**
- **Slide 10A.7.3 slightly modified** to communicate better
- **Slides 10A.7.4 - 16 deleted** (moved to Module 6A: 'Essential PCB EMC')
- **Slides 10A.8.2 and 5 modified** to communicate better
- **Slides 10A.8.3 - 5 renumbered as 10A.8.4 - 6 respectively**

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Change Record: v1.6 – v1.8, January 2019 (2)

- New Slide 10A.8.3 added
- Slide 10A.9.10 updated and split into two slides: 10A.9.10 and 10a
- Slides 10A.9.13, 19 and 30 slightly modified to communicate better
- Slide 10A.10.13 slightly modified to communicate better
- Slide 10A.11.9 slightly modified to communicate better
- Slide 10A.13.22 corrected (both broadside-coupled traces must be on internal layers; and trace widths slimmed down when they enter the field of via holes)
- Slides 10A.13.28, 30 and 35 slightly modified to communicate better
- All the slides in sections 15, 16 and 17 moved to sections 16, 17 and 18 respectively, except for Slide 10A.14.28 renumbered as 10A.15.3
- New Section 15 added, on 3-D Moulded PCBs and Additive Manufacturing
- Section 18 (References and Sources) updated, and web-links added

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Good Electromagnetic (EM) Engineering…

- is cost-effective SI, PI and EMC engineering…
  - well-proven to save time & money in all lifecycle stages, helping to increase profits & reduce financial risks…
  - for PCBs, modules, products, equipment, vehicles, systems, installations, etc., of *any* size, in *all* applications…
  - *see Module 1, especially 1.15 (also in Webinar 1c) and 1.16 (also in Webinar 1d)*

- **This** Module contains many EM Engineering guidelines that should *also* be used as an initial design checklist: *any that can't or won't be followed identify a project risk!*
  - *see Module 1, section 1.16 (also in Webinar 1d)*
- design guidelines based on λ or f_{MAX} are for compliance with IEC 61000-6-1 and -3…
  - to adapt to different EMC standards, see section 1.18 in Module 1: 'The Physics of EMC' *(also in Webinar 1d)*

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Contents

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Contents continued...

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The textbook that this course is based upon

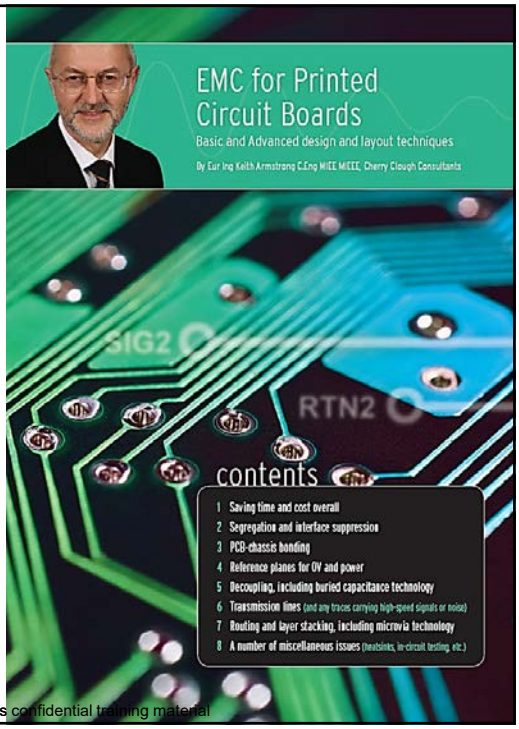
Info and contents list: www.cherryclough.com

Printed-to-Order from:
www.emcstandards.co.uk/books4

***Not* available from Amazon or any other resellers (who might incorrectly state that it is out of print)**

This book was published in 2005 so is not as up-to-date as this course…

but it does provide a lot more detail on the many techniques that haven't significantly changed



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When should we use advanced PCB techniques?

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Advanced PCB techniques help to…

- Reduce cost by eliminating enclosure shielding (or at least reducing its specification and cost)…
- Reduce interference with co-located wireless datacoms (e.g. increase receiver range for GSM, GPRS, 3G, 4G, etc.)…
- Allow co-located GPS antennas…
- Use RF power devices (including isolating DC/DC)…
- Make high-speed processors / DSP function correctly (achieve good signal integrity, SI, and power integrity, PI)…
- Use the latest IC technologies (e.g. 15nm or smaller silicon processes), BGAs and 'chip scale' packages…
- Reduce time to market and compliance costs

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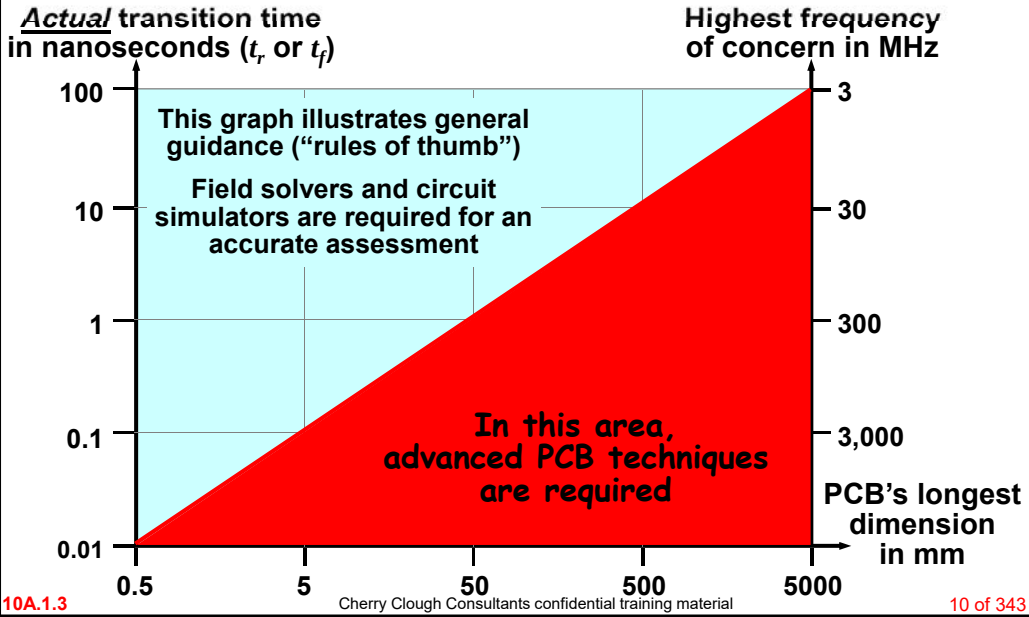
When do we need advanced techniques?



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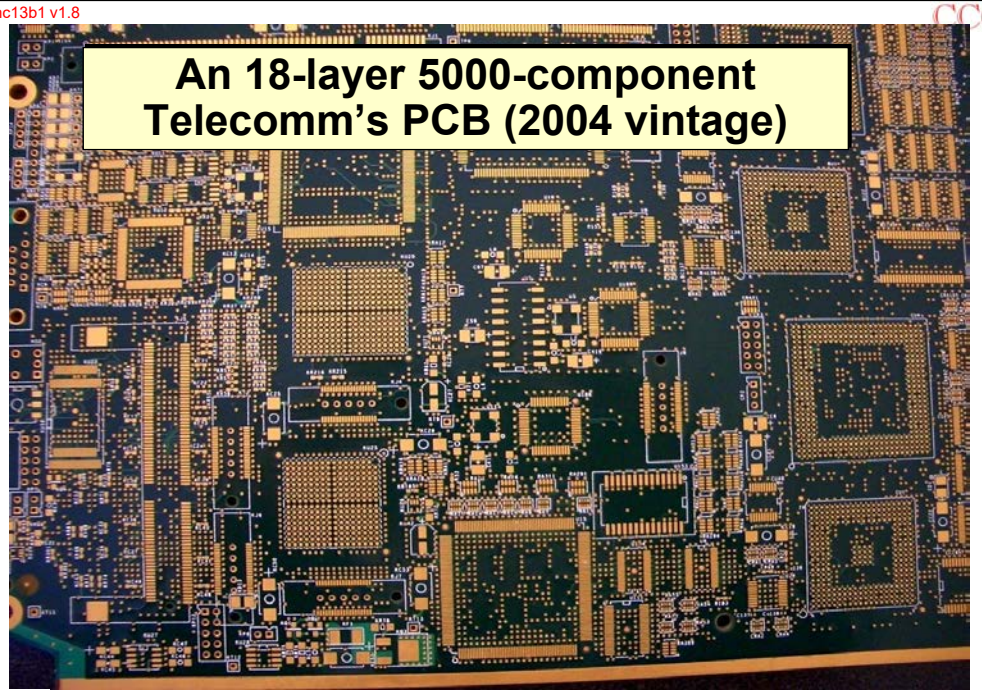
An 18-layer 5000-component Telecomm's PCB (2004 vintage)



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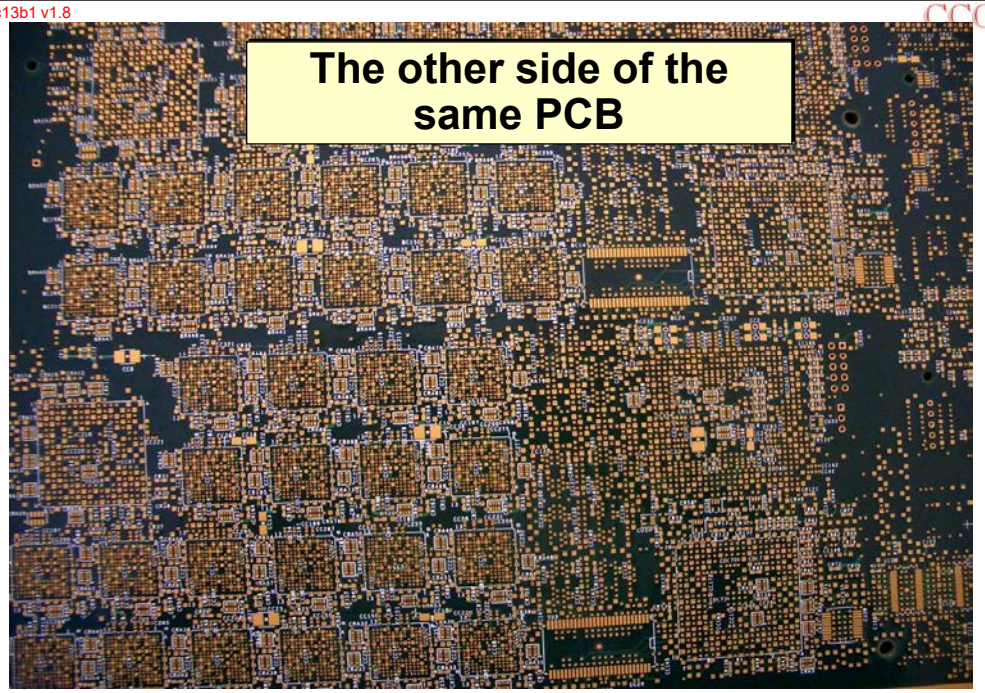
The other side of the same PCB



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Future trends and their implications

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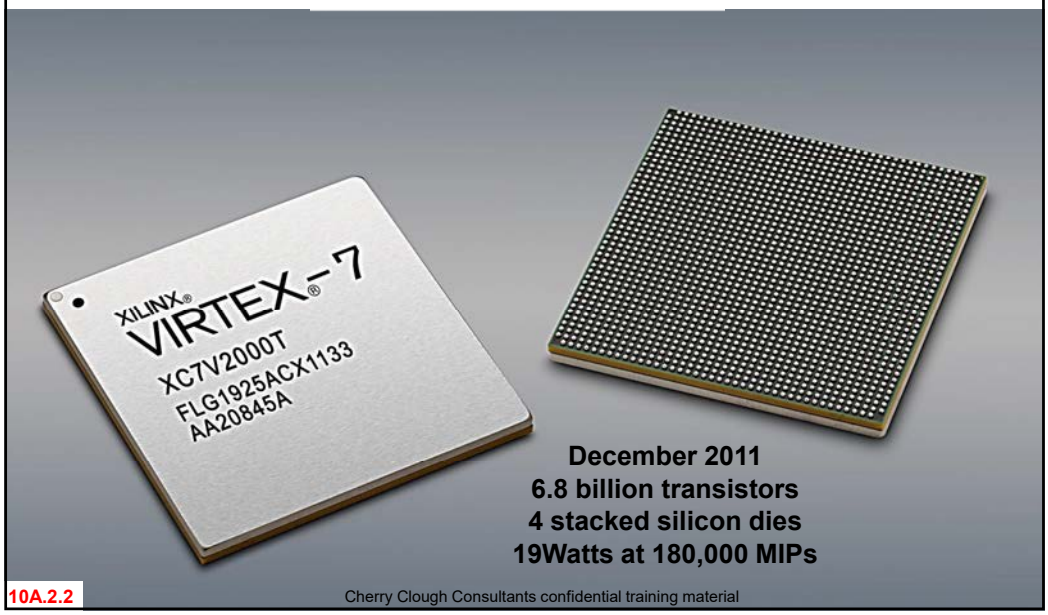
Future trends



December 2011
6.8 billion transistors
4 stacked silicon dies
19Watts at 180,000 MIPs

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IC trends

- **IC trends are driven by:**
  - **increasing processing power...**
  - **increasing complexity (more transistors per square mm)…**
  - **improving wafer yield…**
  - **reducing cost**
- **All these are achieved by shrinking the feature sizes on the silicon wafers…**
  - **now at 15nm, with even smaller processes being developed *(see next)*…**
  - **an unstoppable trend towards smaller feature sizes**

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The ITRS 2007 roadmap

www.itrs2.net

(copied from "Power Integrity and EMC Design for High-speed Circuits Packages", by Prof. Tzong-Lin Wu, Ph.D., National Taiwan University, EMC DL 2009 (IEEE EMC Distinguished Lecture, Netherland/Belgium/Luxembourg Chapter, June 18, 2009)

Year	Feature	V_{dd}	Chip Freq.	Power
2007	68nm	1.1V	4.70GHz	189W
2010	45nm	1.0V	5.88GHz	198W
2013	32nm	0.9V	7.34GHz	198W
2016	22nm	0.8V	9.18GHz	198W
2019	16nm	0.7V	11.48GHz	198W
And from the ITRS 2013 Roadmap:				
2021	12nm	0.74V	7.53GHz	–

April 2018: TSMC is expected to begin 7nm production in June with Qualcomm, Xilinx, Apple, HiSilicon customers. Samsung has just qualified it's first 7nm foundry and expects first products to ship late 2018 / early 2019

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EMC effects of shrinking feature size

- ICs become more susceptible to over-voltage damage…
  - because their insulation is thinner/narrower
- Data 'bits' are more vulnerable to data corruption…
  - due to the wider bandwidth and lower capacitance
- Increasing emissions
  - smaller feature sizes means less capacitance
    - means faster switching edges
    - means more energy in richer harmonic spectra
    - *even if the clock frequency doesn't increase*

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Effects of switching edge speed on the harmonics of a 100MHz clock